

CYPRESS SPARC PROGRAM OVERVIEW

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***Subsidiary of Cypress Semiconductor, Inc.**

SPARC ARCHITECTURE/HARDWARE

- * Based on RISC research done at University of California-Berkeley**
- * Only open multi-vendor RISC architecture**
- * Only RISC architecture with proven system level clone-ability (Solbourne)**
- * Only multi-technology RISC architecture**
 - * Gate array (Fujitsu, LSI)**
 - * Custom CMOS (Cypress, TI)**
 - * Custom BI-CMOS (Cypress)**
 - * ECL (BIT)**
 - * GaAs (Prisma)**

SPARC APPLICATION SOFTWARE BASE

- * Only RISC microprocessor with an operational and demonstrated 'shrink-wrap' software standard
- * The largest software base of any RISC microprocessor, growing at an exponential rate away from the competition (doubling every six months).
- * Over 500 major application programs available as of 2Q89, substantially more than 5X all other RISC microprocessors combined, will exceed 1000 packages by 4Q89
- * World class software covering all major applications of computing:
 - * Office Automation
 - * MS-DOS Emulation
 - * Artificial Intelligence
 - * CASE
 - * Mechanical Computer Aided Design
 - * Project Management
 - * VAX/VMS Emulation
 - * Databases
 - * Manufacturing
 - * Imaging
 - * Mathematics
 - * Financial Services
 - * Electronic Publishing
 - * Electronic Design Automation
 - * Biomedical
 - * Graphics
 - * Earth Resources

CYPRESS SPARC PROGRAM OVERVIEW

- * Architectural Partitioning
- * Product Overview
- * Technology
- * Performance
- * Competitive Analysis
- * Technology Alliances
- * Future Direction

CY7C601-IU

- * **Fully compliant with SPARC reference ISA architecture**
- * **8 register windows**
- * **IEEE Floating-point co-processor interface**
- * **General (user defined) co-processor interface**
- * **Processor bus allows higher clock speed operations (40 and 50 MHz)**
- * **Supports SPARC standard AI data tag operations**
- * **0.8u DLM CMOS**
- * **Clock speed scales to 50 MHz**

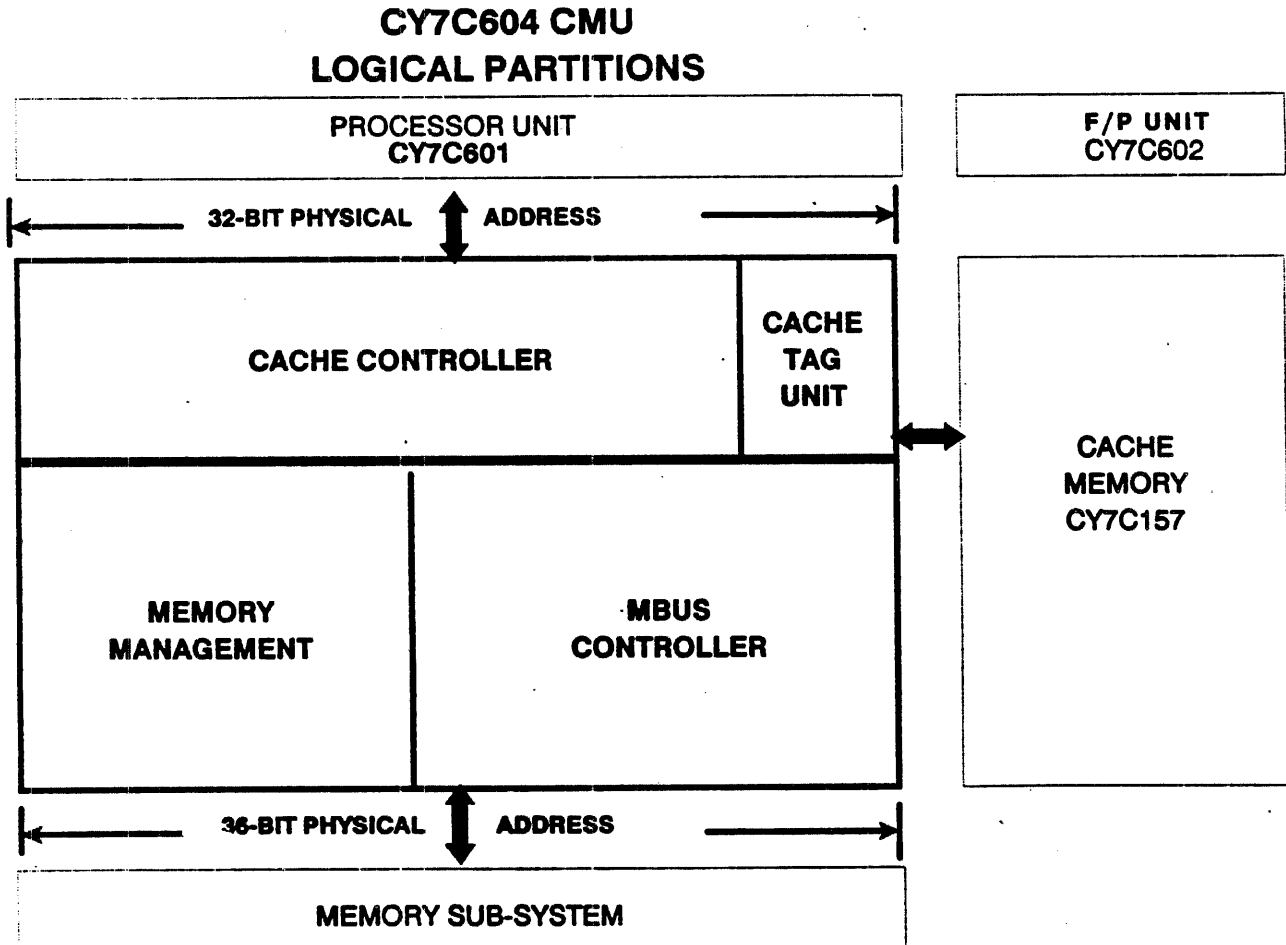
CY7C602-FPU

- * **Single chip with full IEEE double precision floating point hardware combines floating-point control with floating-point processing**
- * **Dedicated register file provides increased overall register bandwidth**
- * **All data paths are 64 bits wide**
- * **Optimal support for real-world floating point problems as characterized by FFT and Lawrence Livermore loop benchmarks**
- * **Clock speed scales to 50 MHz**
- * **Synchronous operation**

CY7C604 - CMU

Features:

- * Integrated architecture
 - * Cache tag unit
 - * Cache controller unit
 - * SPARC standard Memory Management Unit
 - * SPARC standard 64-bit Mbus control unit
- * Interfaces directly to zero-wait state CY7C157 cache rams
- * Cache size is expandable to meet systems requirements (64K->256K)
- * Clock speed scales to 50 MHz
- * Synchronous operation



CY7C604 MEMORY MANAGEMENT UNIT

- * Fully compliant with "The SPARC reference MMU architecture" specification
- * 32-bit virtual address (4G-byte)
- * 36-bit physical address (64G-byte)
- * 4096 multiple contexts (task ID's)
- * 4k-byte page size
- * Lockable 64-entry fully associative TLB
- * Memory address protection checking
- * Hardware table walk
- * Support for sparse address spaces with 3 level map

CY7C604 CMU CACHE CONTROLLER UNIT

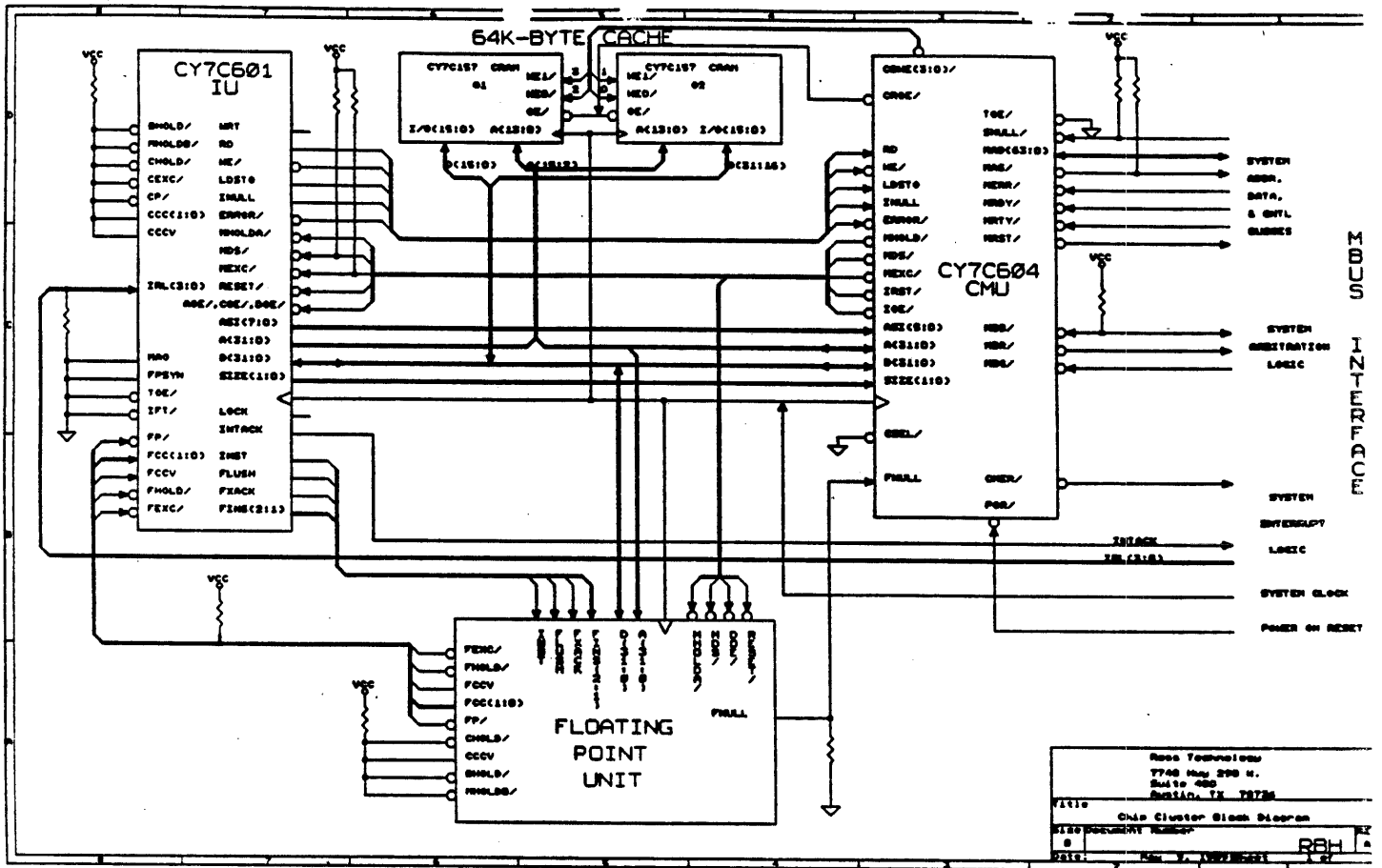
- * 2K direct mapped virtual cache tag entries
- * Write-through and copy-back modes
- * 32 byte cache line size (8 instructions)
- * Full cache-line write buffer
- * Full cache-line read buffer
- * Address Aliasing (synonym) detection
- * Byte-write enables
- * Cache lock

CY7C604 SUB-UNIT MODULE BUS UC

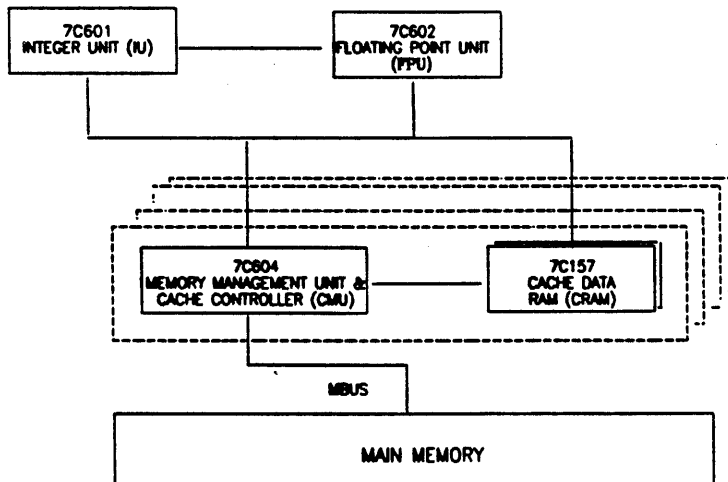
- * **Fully synchronous bus**
- * **All signals changed and sampled on rising clock edge**
- * **64-bit multiplexed address/data**
- * **Multiple - Master Bus**
- * **Overlapped Arbitration**
- * **320 M bytes/second peak transfer at 40 MHz**
- * **5 cycle burst transfer cache line refill**

CY7C157 - CACHE MEMORY UNIT

- * **Custom design for CY7C604 cache applications**
- * **256K SRAM technology base**
- * **Idealized cache aspect ratio (16K x 16)**
- * **On chip address and data latches**
- * **Self-timed write**
- * **52 pin plastic leaded chip carrier**
- * **Clock speed scales to IU and CMU**
- * **Synchronous operation**



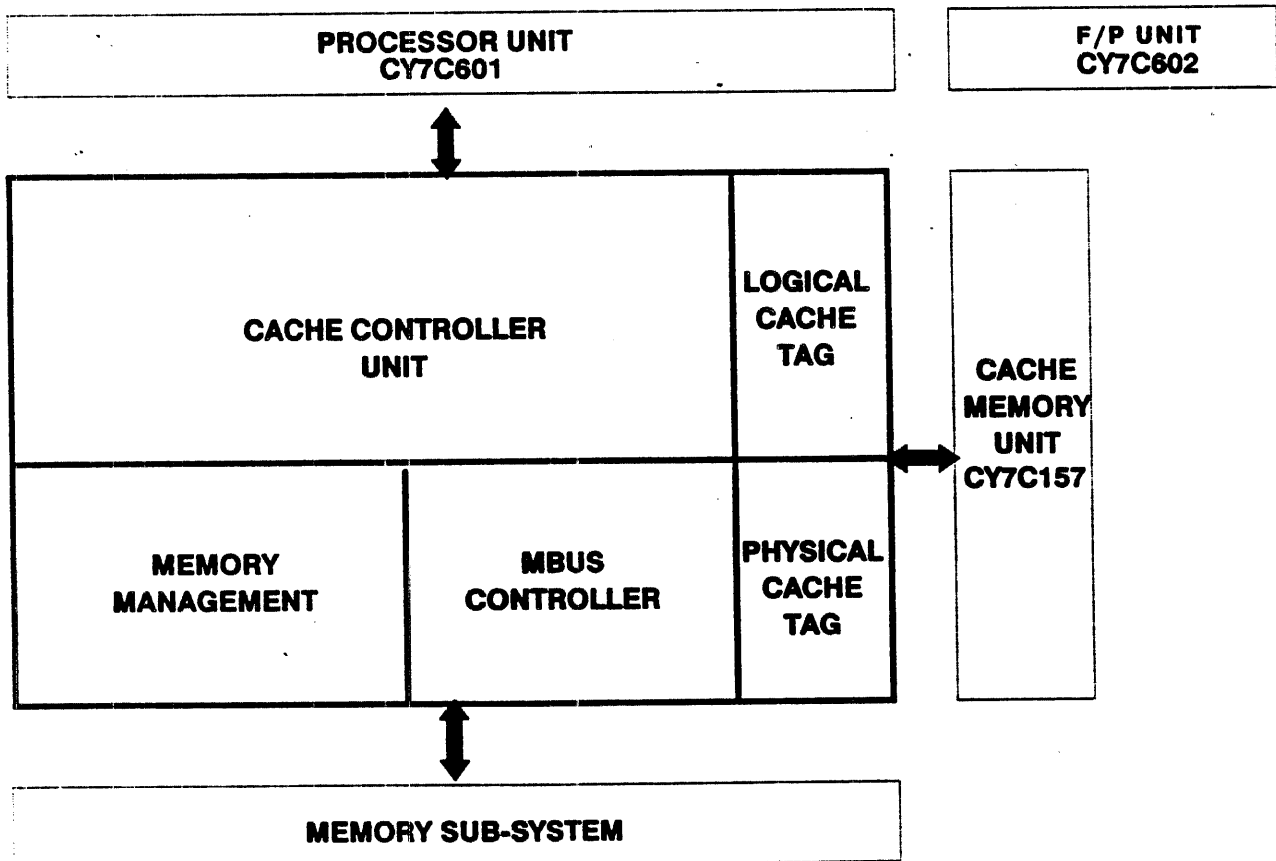
EXTENSIBLE CACHE
64 - 256 KB



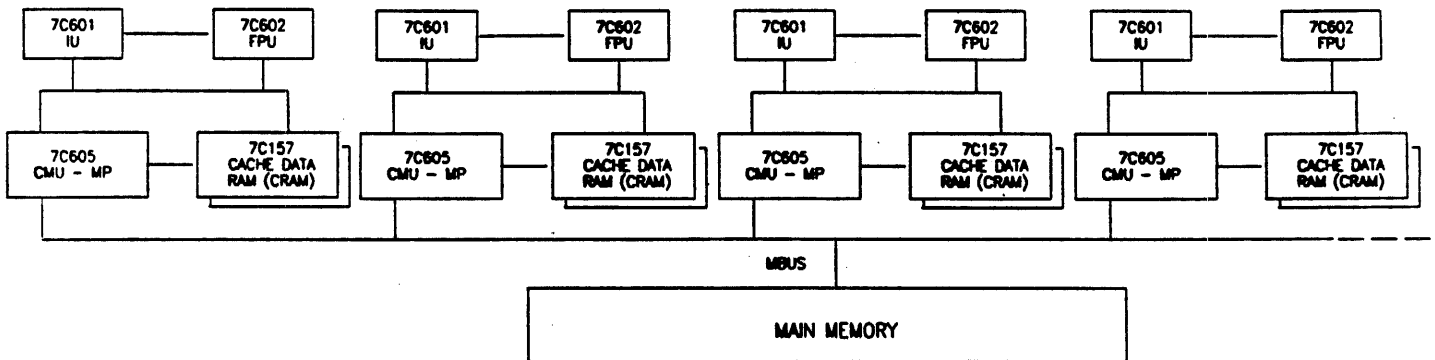
CY7C605 - CMU - MP

- * Includes all features and functions of the 7C604
- * Additional physical cache tag of 2K entries for concurrent tag access
- * No real-time degradation due to bus watch operations
- * Future bus "MOESI" cache consistency model support (modified, owned, exclusive, shared, invalid)
- * Direct data intervention support
- * Reflective memory operations support
- * Complementary-set secondary cache support
- * Clock speed is scalable with IU
- * Synchronous operation

CY7C605 CMU - MP LOGICAL PARTITIONING

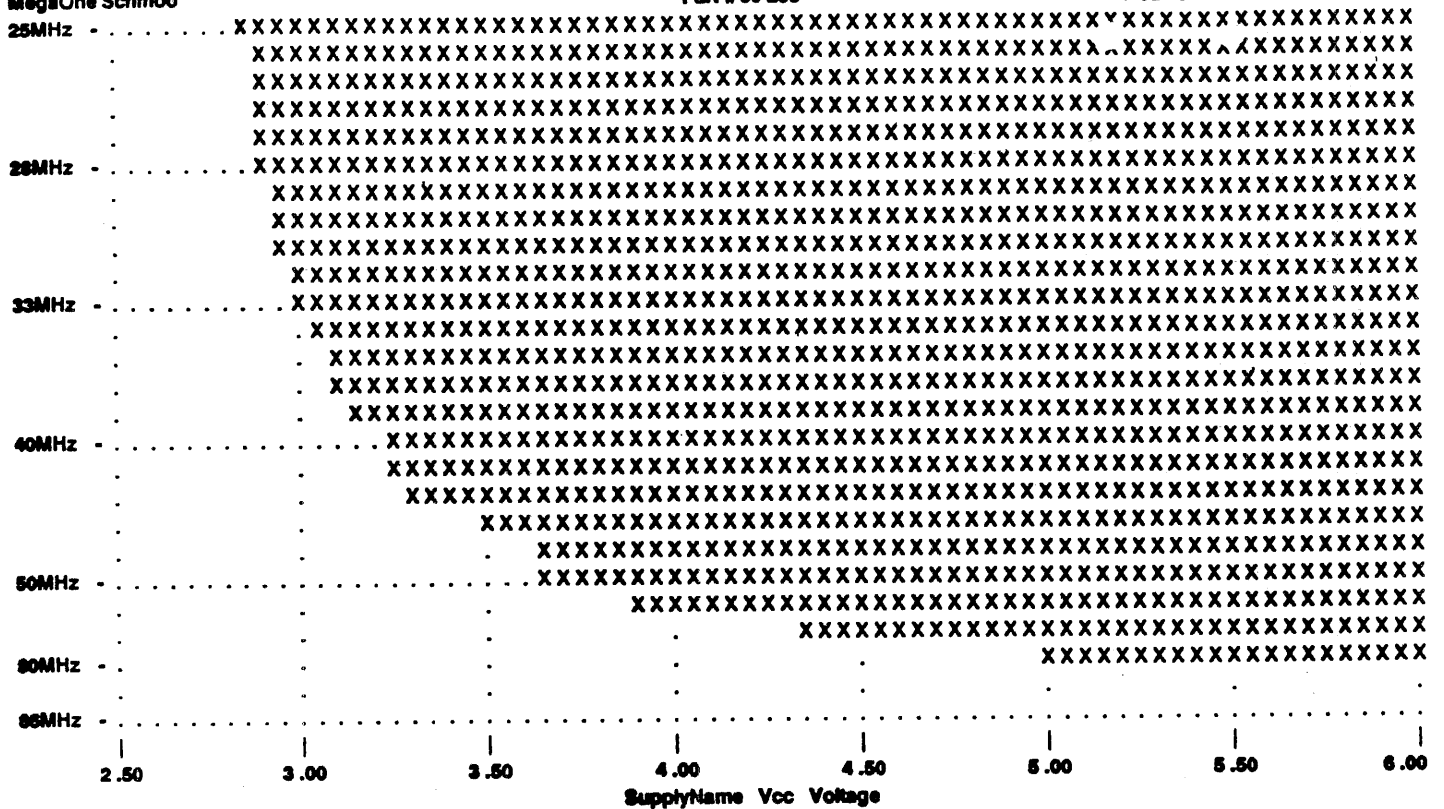


ARCHITECTURAL PARTITIONING (MULTI-PROCESSING WITH 4 PROCESSOR MODULES)



CYPRESS CMOS TECHNOLOGY LEADERSHIP

- * 0.8 micron Double Layer Metal CMOS
- * 0.65 "L effective"
- * Based on high speed Cypress 256K SRAM technology
- * 33 MHz initial frequency of operation
- * 50+ MHz devices at maturity
- * 2 to 3 generations ahead of competition



COMPETITIVE ANALYSIS

	Cypress 7C600	AMD 29000	Motorola 88000	MIPS R3000	Intel 860
General					
Implementation	0.8u CMOS	1.2u CMOS	1.5u->1.2u CMOS	1.2u CMOS	1.0 u CMOS
Clock Frequency	33->80 MHz	16->25 MHz	20->25 MHz	16->25 MHz	33->80 MHz
(VAX MIPS) Performance	24->36 MIPS	11->18 MIPS	15->19 MIPS	13->20 MIPS	15->22 MIPS
Cache					
Large-Scale Register Files	136 Registers (Windows)	182 Registers (Back Cache)	None	None	None
Scalable cache system	Yes	None	Yes	None	None
Secondary Cache Support	Yes	None	None	None	None
Cache Extensibility	(64->286k)	None	(32->128k)	None	12k
Multiprocessing Support	Yes	None	Yes	None	None
Cache Coherency	Yes - Real-time direct	None	Yes - Non real- time indirect	None	None
Semaphore Support	Yes	Yes	Yes	None	Partial
Cache Locking	Yes	No	No	No	No
Floating Point					
Hardware Double Precision	Yes	Yes	No (32 bit)	Yes	No (32 bit)
Dedicated Floating Point Register File	Yes	No	No	Yes	Yes
Synchronous Operation With IU	Yes	No (Decoupled)	Yes	Yes	Yes

CYPRESS 7C600 TECHNOLOGY ALLIANCES

- * **We will coordinate with the other SPARC licensees to help promote the SPARC architecture as the RISC computing standard:**
 - * **TI**
 - * **Bit**
 - * **Fujitsu**
 - * **LSI Logic**

- * **Texas Instruments Partnership**
 - * **The first true SPARC second source**
 - * **A 5 year alternate source agreement covering all members of the 7C600 family**

CYPRESS' FUTURE DIRECTIONS

- * **Scale the current CY7C600 chip set to 40 MHz in 1989 and 50 MHz in 1990**
- * **M-Bus based SPARC-module integrated product for 50 MHz operation**
- * **M-Bus based peripheral support chips**
- * **Produce derivatives optimized for specific market segments - embedded control, real-time, vector FP, etc. . . .**

SPARC-MODULE

- * Provides 50 MHz Operation Speeds For Present Cypress Product Line**
- * Integrates (601, 602, 604, 605, 157) Into A Single Mini-Board Product**
- * Provides Single and Multi-Processor Options**
- * Tightly Controlled Capacitance And Clock-Skewing**
- * Extensible Cache Sizes**
- * Multi-layered PCB With Standard M-Bus Interface**
- * Plug Compatible (PGA) Single-Processor Version Can Be Replaced By Next Generation Integrated Processor Chip At The Field Level**