

# Hot Chips 11

A Symposium of High-Performance Chips

Sunday, August 15, 1999 - Tuesday, August 17, 1999

Memorial Auditorium  
Stanford University

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Sunday, August 15, 1999

## Tutorial I: Digital Signal Processing

*Chair: Teresa Meng*

### *Video Algorithms and Architectures*

*Dr. Kees A. Vissers, Philips Research*

### *Signal Processing in Communications I: xDSL*

*Dr. Sam Sheng, DataPath Systems*

### *Signal Processing in Communications II: CDMA*

*Dr. Sam Sheng, DataPath Systems*

## Tutorial II: IA64 Architecture and Compilers

*Chair: Ken Shoemaker*

### *IA-64 Architecture Basics/Introduction*

*Dr. Allan Knies, Intel*

### *Optimization Techniques/Using IA-64 Features*

*Dr. Allan Knies, Intel*

### *Compiler Technology on IA-64*

*Dr. Jesse Fang, Intel*

# *Dynamic Compilation Technology on IA-64*

*Dr. Jesse Fang Intel*

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Monday, August 16, 1999

## Welcome, Opening Remarks

*General Chair: Michael Blasgen*

*Program Co-Chairs: Forest Baskett, Monica Lam*

## Session 1: Parallel Machines

*Session Chair: John Kubiatawitz*

### *A Multi-Threaded 64-bit PowerPC Commercial RISC Processor Design*

*S. Storino, J. Borkenhagen, IBM*

### *A RISC Processor for SR8000: Accelerating Large Scale Scientific Computing with SMP*

*Y. Tamaki, T. Kurihara, K. Shimada, E. Kamada, T. Shimizu, Hitachi*

### *The Stanford Hydra CMP*

*L. Hammond, B. Hubbert, M. Siu, M. Prabhu, M. Willey, M. Chen, M. Kozyczak, K. Olukotun, Stanford University*

## Session 2: New Technology

*Session Chair: Peter Hsu*

### *A 1GHz Power4 Testchip Design*

*B. McCredie, J. Badar, R. Bailey, P. Chou, C. Carter, D. Ervin, M. Floyd, J. Keaty, B. Krauter, J. LeBlanc, L. Leitner, D. Mikan, Jr., M. Nealon, J. Petrovick, K. Reick, P. Restle, T. Skergan, H. Stogdon, J. Vargus, J.D. Warnock, IBM*

### *A Synchronous Wave-Pipeline Interface*

*E. Cordero, D. Dreps, F. Ferraiolo, M. Floyd, K. Gower, B. McCredie, IBM*

### *A Field-Sequential Color 1040 by 768 Liquid Crystal on Silicon Display*

*Michael Bolotski, The MicroDisplay Corporation*

## Keynote: New Millenium for Computer Entertainment

*Ken Kutaragi, President, Sony Computer Entertainment*

*Chair: Mitsuo Saito*

## Session 3: Graphics Processors

*Session Chair: Henry Moreton*

### *5.5 GFLOPS Vector Units for Emotion Synthesis*

*A. Kunimatsu, N. Ide, T. Sato, Y. Endo, H. Murakami, T. Kamei, M. Hirano, M. Oka, A. Ophba, T. Yutaka, T. Okada, M. Suzuoki, System ULSI Engineering Laboratory of the Toshiba Corporation, Sony Computer Entertainment.*

### *Massively Parallel SIMD Computing on a Single Chip*

*R. McConnell, PixelFusion*

### *MAP1000A: a 5w, 230 MHz VLIW Mediaprocessor*

*J.O'Donnell, Equator*

## Session 4: Embedded Machines

*Session Chair: Howard Sachs*

### *High Speed Low Cost TM1300 Trimedia Enhanced PCI VLIW Mediaprocessor*

*L. Lucas, Philips Semiconductors*

### *The ARM9TDMI and ARM9ESP Synthesizable Families*

*A. Burdass, ARM*

### *Configurable/Extensible Processors Change System Design*

*R. Gonzalez, Tensilica*

## Panel: Information Appliances in the Home

*Panel Chairs: Norm Jouppi and Ken Shoemaker*

*Moderator: Kathy Richardson - Compaq Computer / Institute for Women and Technology*

*Panelists: David Armitage, President Qubit*

*Jim Barton, CTO, TiVo*

*Natasha Flaherty, Market Manager, Asia, Phone.com*

*Elizabeth Houck, Philips Research*

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Tuesday, August 17, 1999

## Session 5: PC and Special-purpose Chips

*Session Chair: Gert Slavenburg*

### *IGR4-A High Performance AMD K7 Northbridge w/ RDRAM Memory Controller*

*C. Keltcher, J. Kelly, R. Krishnan, J. Peck, S. Polzin,  
S. Subramanian, F. Weber, AMD*

### *High-Performance Sort Chip*

*S. Azuma, T. Sakuma, T. Nakano, T. Ando. K.  
Shirai, Mitsubishi*

### *The vg500 Real-Time Ray-Casting ASIC*

*H. Pfister, Mitsubishi Electric Research Laboratory*

## Session 6: Software

*Session Chair: Marc Tremblay*

### *Virtual Platform-A Virtual Machine Monitor for a Commodity PC*

*M. Rosenblum, VMware*

### *Wiggins/Redstone-An On-line Program Specializer*

*R. Gordon, Compaq*

### *Hardware Support for Out of Order Instruction Profiling on Alpha 21264a*

*J. Anderson, L. Berc, J. Dean, S. Ghemawat, S.  
Leung M. Litchenberg M. Vandevoorde, G. Verns,  
C. Waldspurger, W. Wehl, J. White, Compaq*

## Keynote: Broadband Communications IC's for High-Speed Networking in the Home

*Henry Samuelli, Co-Chairman and Chief Technical  
Officer, Broadcom*

*Chair: John Hennessy*

## Session 7: Network Chips

*Session Chair: Earl Killian*

### *The Epigram EPI41210/EPI41100 16bps Home Phoneline Networking Chipset*

*A. Corry, G. Efland, E. Frank, N. Ferrario, H. Garlapati, R. Hayes, J. Holloway, H. Kuo, J. Laudon, T. Mallory, W. Morton, G. Loyola, N. Nucklos, J. Pattin, H. Ptasinski, K. Peterson, E. Ojard, D. Snow, W. Stafford, T. Robinson, J. Trachewsky, L. Yamano, C. Young C. Warth, R. Alva, B. Bunch, D. Fifield, N. Castagnoli, M. Dove, M. Kobayashi, R. McCauley, S. Mohapatra, T. Moorti, A. Siddeqee, W. Shieh, S. Siener, Epigram*

### *Broadcom BCM5600 StrataSwitch: A Highly Integrated Ethernet Switch On A Chip*

*A. Essen and James Mannos, Broadcom Corporation*

### *SiRFstar II Architecture: A Powerful System Platform for Consumer GPS Application*

*G. Turetzky, J. Knight, R. Tso, L. Peng SiRF Technology*

## Session 8: Instruction Sets

*Session Chair: Alan Smith*

### *An Architecture Extension for Efficient Geometry Processing*

*R. Thekkath, MIPS Technologies*

### *An Architecture for the New Millenium*

*M. Tremblay, Sun Microsystems*

### *The Internet Streaming SIMD Extensions*

*S. Thakker, Intel*

## Closing Remarks