



# JIO : High Performance I/O & Graphics For UltraSPARC IIIi-based Systems

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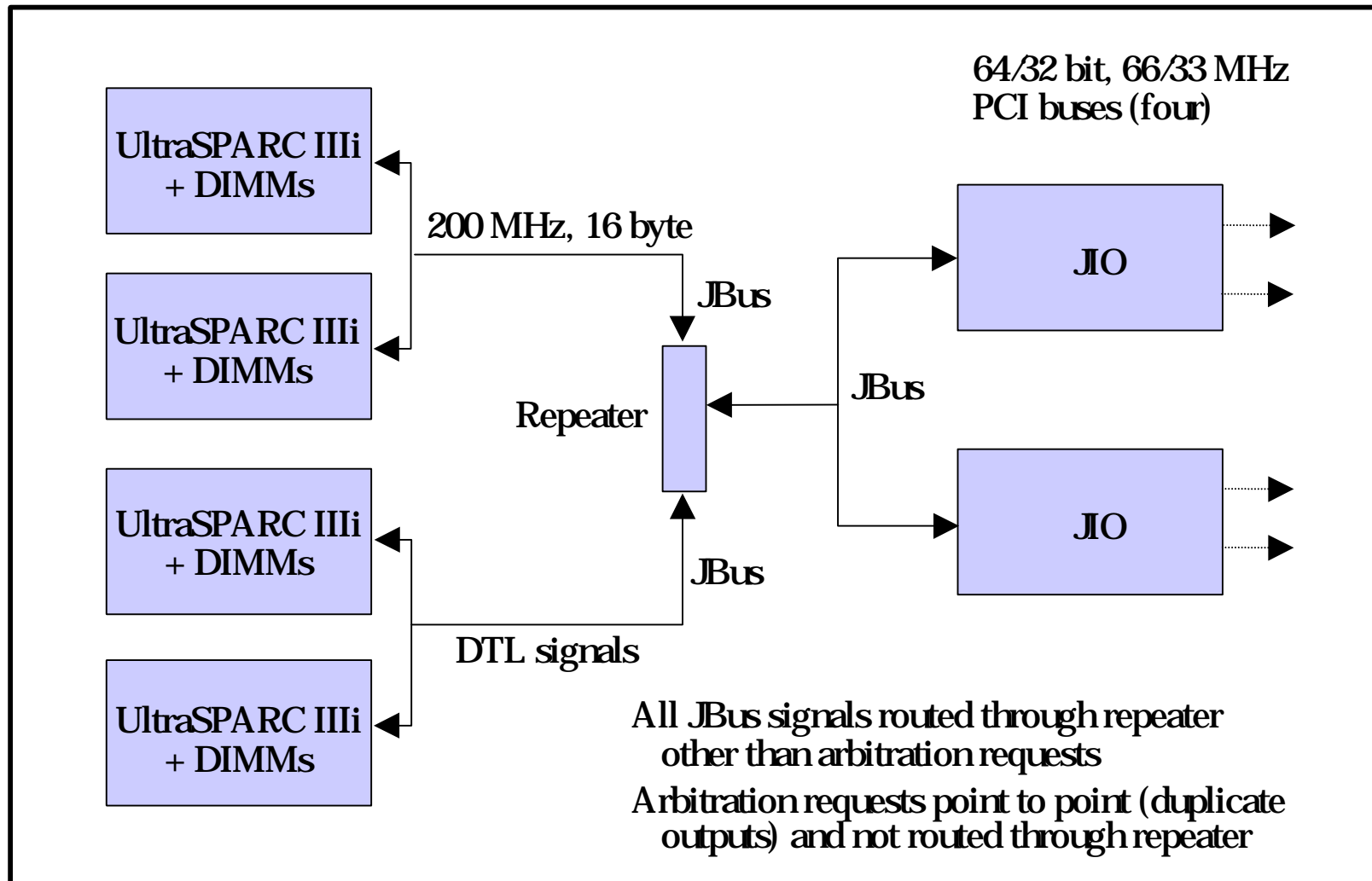
**Processor & Network  
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# I/O Design Goals

- Integrate high-bandwidth, low latency interfaces on single chip :
  - Industry standard PCI I/O and Sun UPA 64S Graphics
  - Reduce system complexity/cost
- Interface with JBUS system bus
- Support 1 - 4 way UltraSPARC IIIi-based multiprocessor systems
- Generate system reset
- Binary compatibility with Solaris and I/O Drivers

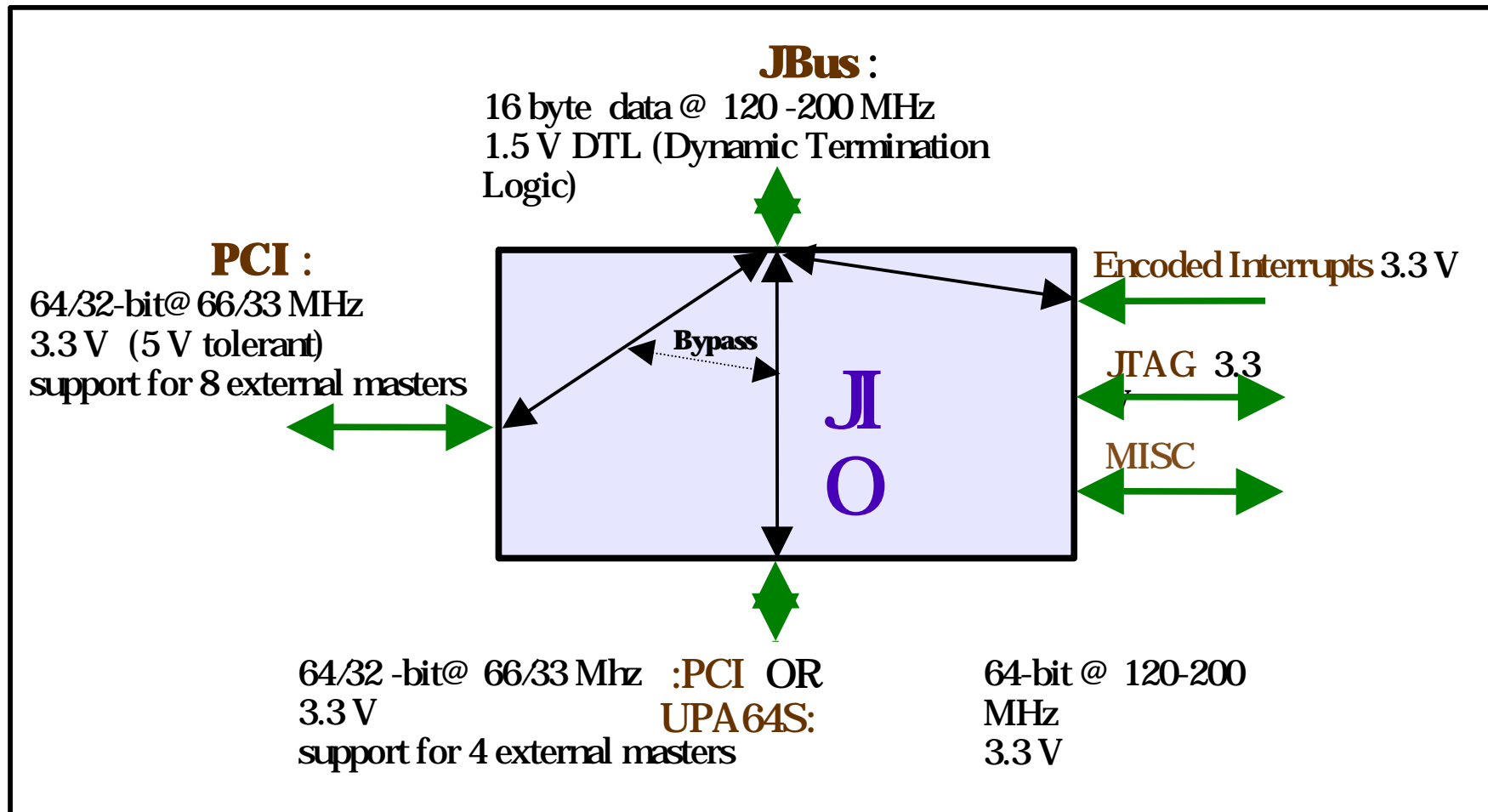
# UltraSPARC IIIi 4-way SMP



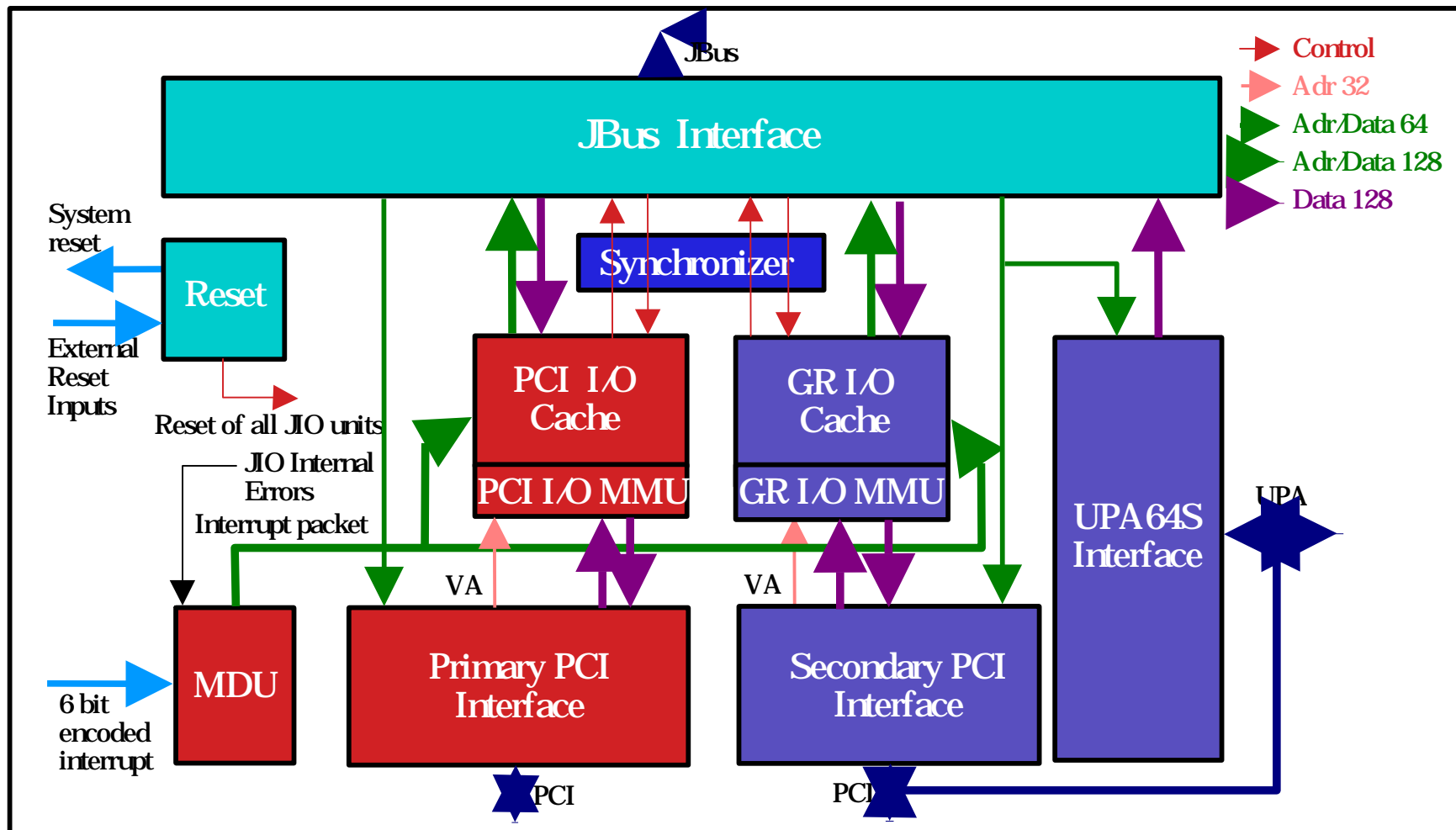
# JBus Features

- . 16 byte split transaction shared address/data bus
  - . Operating speeds up to 200 MHz
  - . Peak bandwidth of 3.2 GB/s
- . On-chip MOESI protocol with decoupled cache snooping
- . Distributed round-robin arbitration favoring last port driver
- . Low pin count (179 DTL signals)
- . Support for out-of-order data return to source
- . Simple point-to-point snoop result propagation
- . Separate flow control (encoded) for address and data
- . Parity protection for data and control
- . Globally synchronous clocking

# JIO Interface/Data Flow View



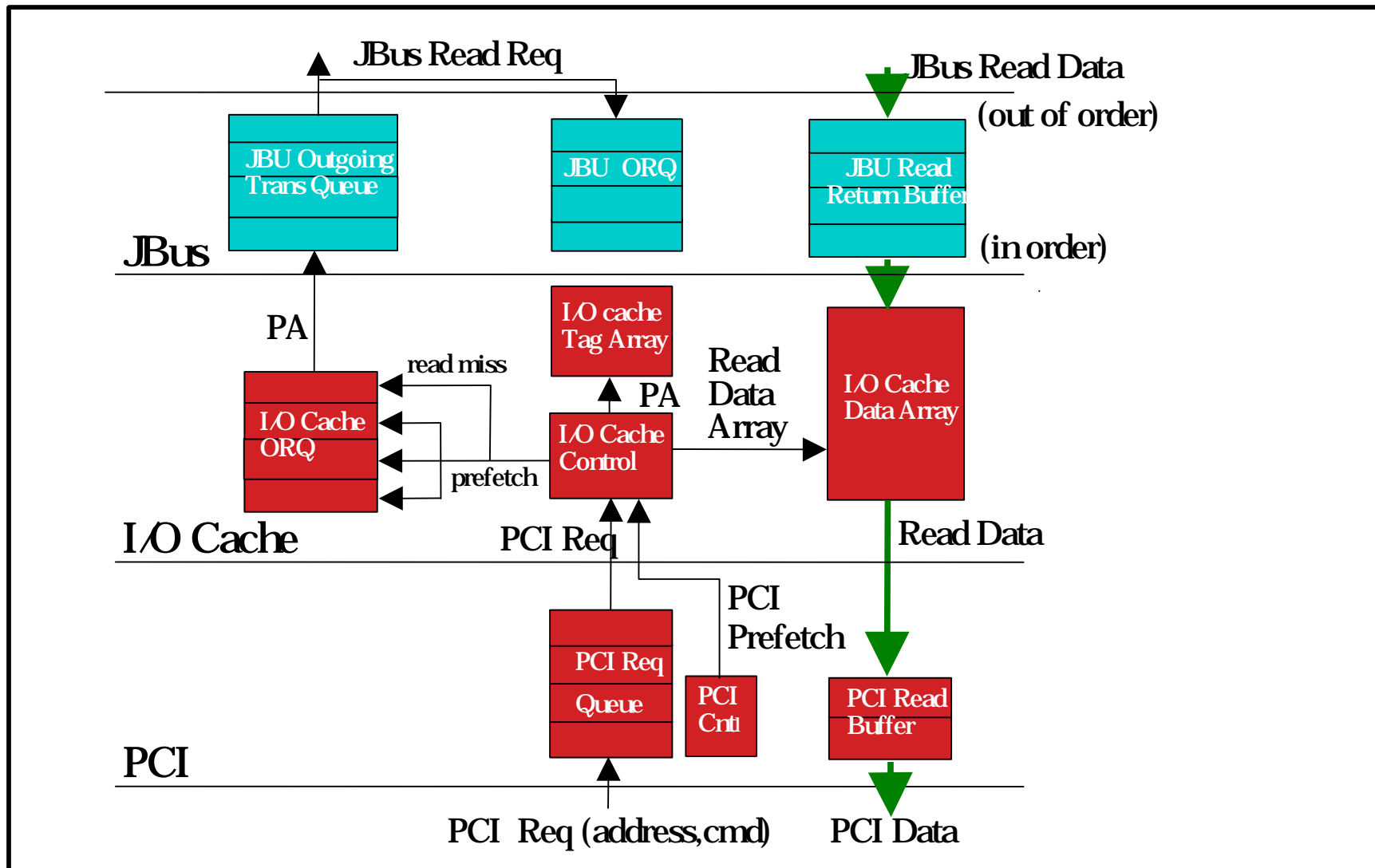
# Block Diagram



# Clock Domain Details

System Interfaces	Clock Domains
<p>JBus : 1.5 V DTL</p> <p>16 byte bit shared address/data 120 – 200 MHz clock 179 signal pins</p>	<p>JBus PLL with PECL differential JBus system clocks as reference</p> <p>100 – 200 MHz lock /operation range</p>
<p>Primary PCI : 3.3 v (5 v tolerant) LVTTL</p> <p>64/32 bit shared address/data 25 – 66 MHz clock 103 signal pins</p>	<p>Primary PCI PLL with single ended full range swing PCI reference clock signal</p> <p>25 – 66 MHz lock range 100 – 133 MHz range of operation</p>
<p>Secondary PCI/UPA 64S Graphics :</p> <p>3.3 v LVTTL 113 signal pins multiplexed PCI : 25 – 66 MHz clock UPA : 120 – 200 MHz clock</p>	<p>Graphics PLL which can be selectively configured as :</p> <p>PCI : Single ended full range swing PCI reference clock signal 25 – 66 MHz lock range 100 – 133 MHz range of operation UPA : PECL differential UPA system clock as reference 100 – 200 MHz lock/operation range</p>

# I/O Cache and PCI Prefetch Pipe



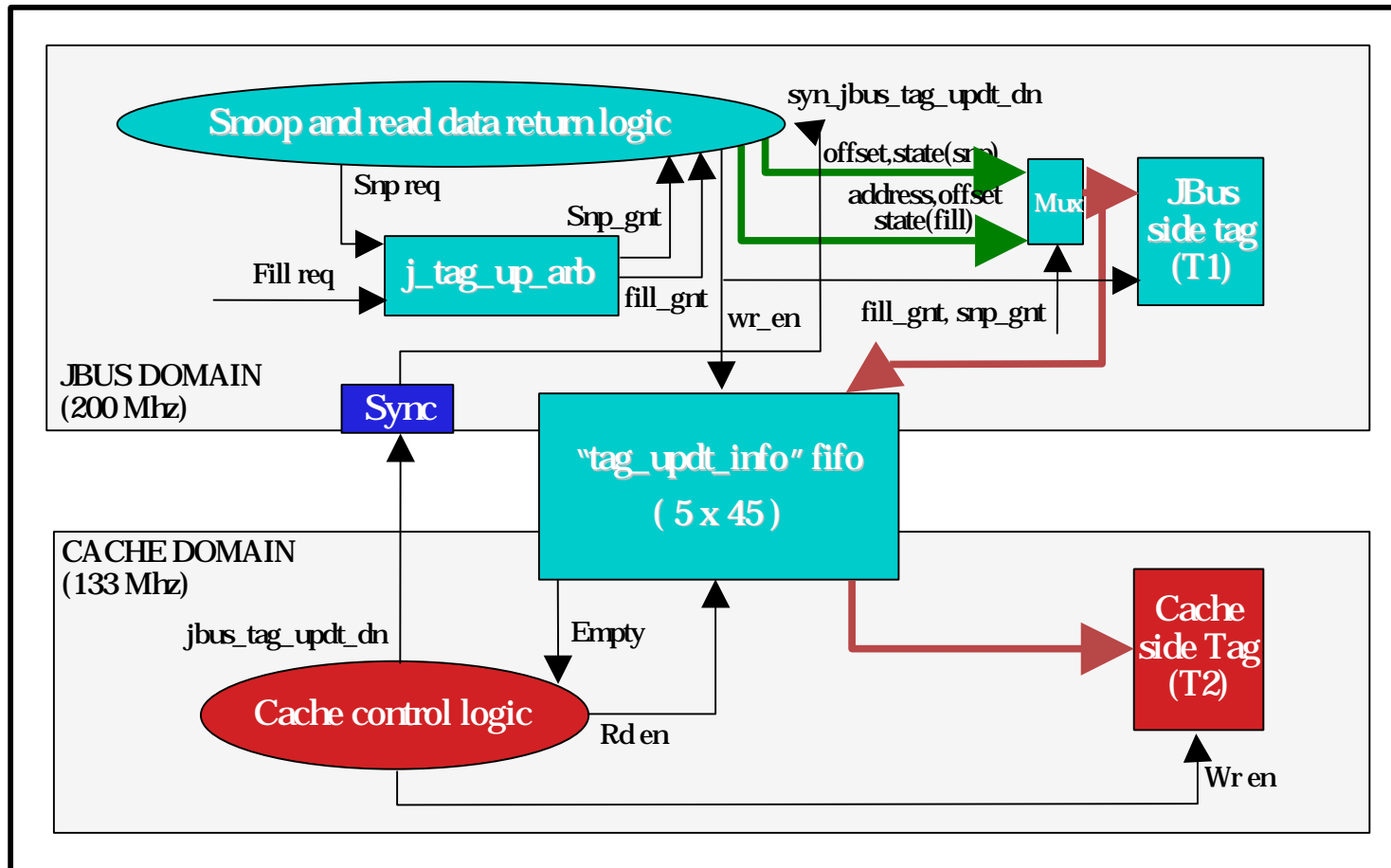
# JBus Unit

- . Provides JIO's interface to JBus
- . Operational frequency of up to 200 MHz
- . Responds to CPU snoops in 3 JBus cycles for all cases other than invalidates
- . Maintains a copy of I/O cache tags
- . Peer-peer arbitration ONLY at JBus level
- . Supports up to 4 outstanding reads per cache

# I/O Cache Unit

- Serves as prefetch buffer fully coherent with main memory
- Fully set associative cache memory of 8 lines of 64 bytes
- Maximum operational frequency of 133 Mhz
- Uses Read-Modify-Write /Write-back write policy for < 64 byte writes
- Bypasses cache to memory for 64 byte (cache line) writes
- FIFO-like counter-based replacement policy
- CSR-enabled prefetch of 1,2,3 cache lines for PCI commands
- CSR-enabled prefetch stride of 1 - 127 cache lines within 8K page
- Prefetch both on a hit or miss

# JBus - I/O Cache Coherency



# PCI Unit

- . Provides JIO's interface to industry-standard PCI bus (2.2 spec)
- . Internally Breaks up DMA transactions at 64 byte (cache line) boundaries
- . Two-level low and high priority round-robin PCI bus arbitration scheme
- . CSR - enabled prefetch of 1 cache lines for PCI commands
- . Two-cache line deep data buffer enhances DMA read performance

# UPA Interface Unit

- . Provides JIO's interface to Sun UPA 64 system bus
- . Enhanced Sun 2.0 Unified Port Architecture
- . Master interface only
- . Operational speed of 100 to 200 Mhz (UPA 64S clock domain)
- . Maximum of 16 total outstanding transactions
  - . Up to 4 reads and 12 writes
  - . Up to 16 writes (no reads)

# I/O Performance

- 2 GB/s system I/O bandwidth (with 2 I/O chips)
- Uninterrupted reads and writes from PCI cards (64-bit/66 MHz!)
- Peak PCI performance for short bursts (32 or 64 bytes)
- UltraSPARC IIIi can saturate PCI and UPA with PIO stores (4, 8, 16, 64 bytes)
- Hardware table walk for IOMMU miss

PCI DMA, 64-bit @ 66 MHz, 1 master

Burst Size (bytes)	DMA write (MB/s)	DMA read (MB/s)
32	301	162
64	384	248
128	444	281
1024	515	465
8192	515	465

PCI Memory PIO, 64-bit @ 66 MHz

Burst Size (bytes)	PIO write (MB/s)	PIO read (MB/s)
4	88	62
8	106	106
16	211	211
64	384	384

UPA Store Throughput, JBus @ 200 MHz

Burst Size (bytes)	UPA Bus Frequency		
	200 MHz (MB/s)	150 MHz (MB/s)	100 MHz (MB/s)
<b>8</b>	<b>1.55</b>	<b>1.12</b>	<b>0.80</b>
<b>16</b>	<b>1.50</b>	<b>1.20</b>	<b>0.80</b>
<b>64</b>	<b>1.32</b>	<b>1.12</b>	<b>0.80</b>

# JIO Implementation

- . ASIC Gate Count : 922 K
- . Memory Storage : RA - 55 K, Flops – 29 K
- . Die Size : 9.5 mm. sq.
- . Signal Pins : 433
- . Package : 728 pin FCPBGA
- . Max. Power Consumption : 10 Watts
- . Technology : 0.25 Micron CMOS

Q & A