

# An Asynchronous SoC Interconnect

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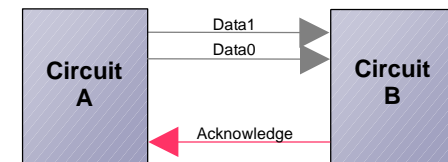


# Agenda

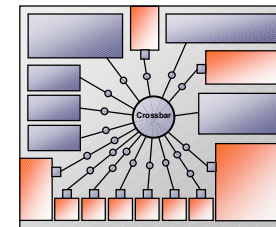
- Introduction to Fulcrum



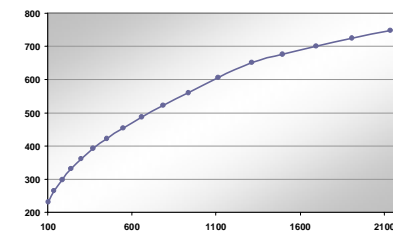
- Asynchronous Technology Overview



- Asynchronous SoC Interconnect



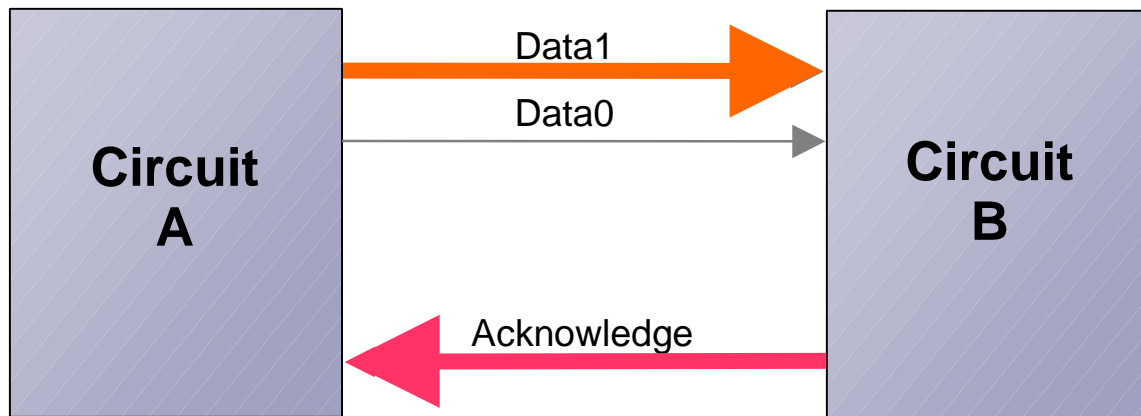
- F1 Project Characterization Results



# Asynchronous Design Styles

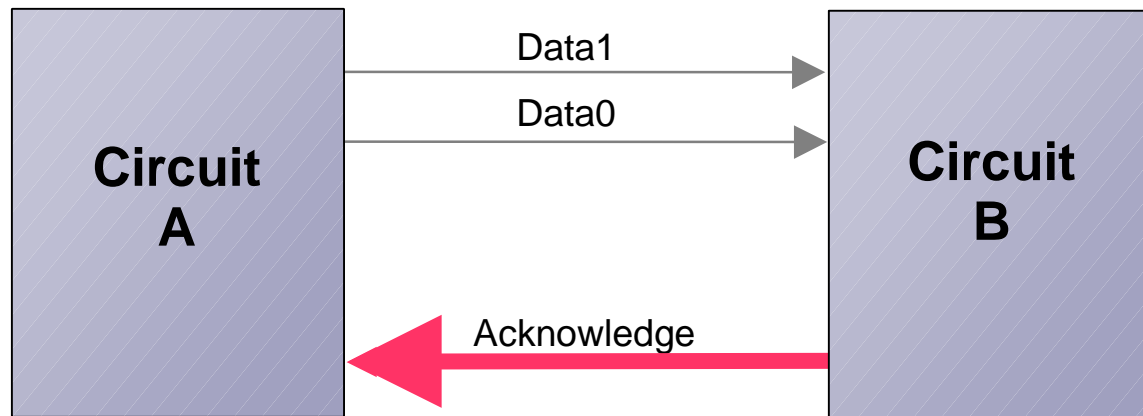
- **Fundamental Mode (1950s)**
  - Predates invention of the clock (combinational logic with feedback)
- **Bundled Data (aka Micro-pipelines) (1989)**
  - Proposed by Ivan Sutherland at Sun Labs
  - Synchronous style datapath, asynchronous control
- **No-Holds-Barred Asynchronous (1995-present)**
  - Self timed with aggressive timing assumptions
  - Mixture of strategies; not a uniform methodology
- **Delay Insensitive (1960s, 1985-1994)**
  - Early MIT and later Caltech research
  - Dynamic logic, similar number of N and P transistors, separate latches
- **Integrated Pipelining (1994-present)**
  - Developed at Caltech by Fulcrum's founders
  - Fast Delay-Insensitive style using domino logic without latches

# Dual-Rail Four-Phase Handshake



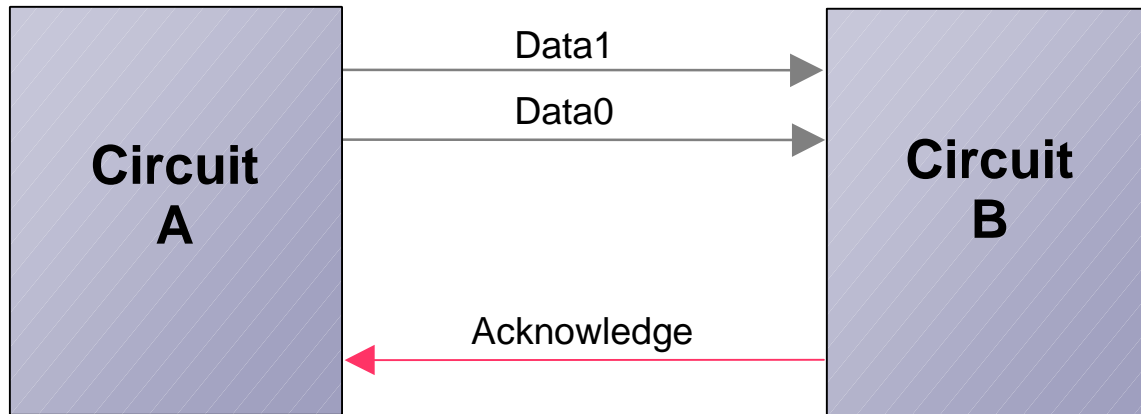
- 1 A raises Data0 or Data1
- 2 B raises Acknowledge

# Dual-Rail Four-Phase Handshake



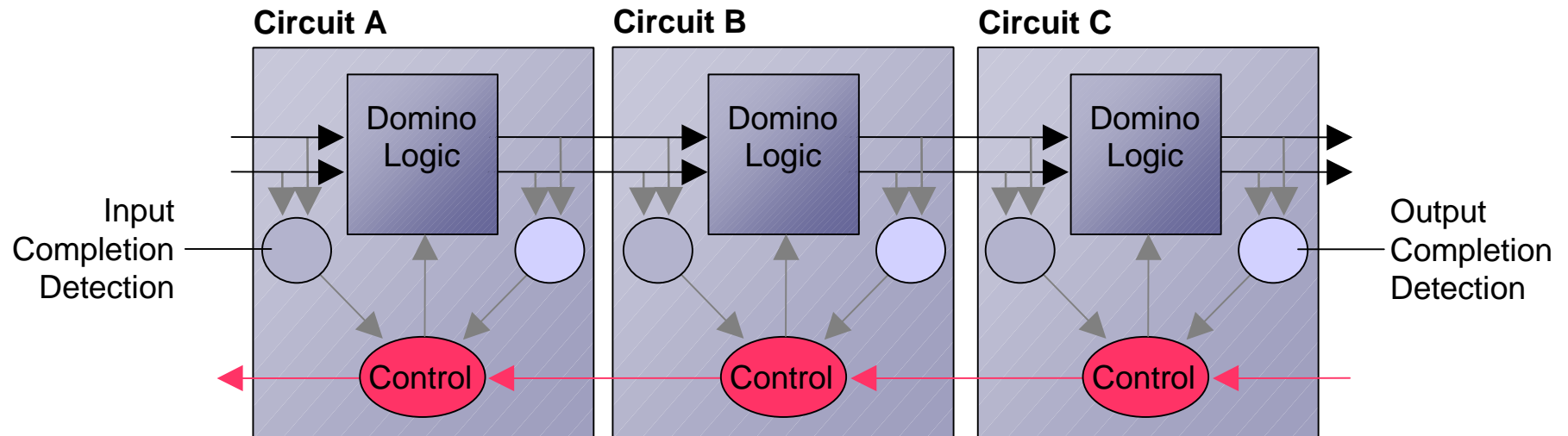
- 1 A raises Data0 or Data1
- 2 B raises Acknowledge
- 3 A lowers Data0 and Data1

# Dual-Rail Four-Phase Handshake



- 1 A raises Data0 or Data1
- 2 B raises Acknowledge
- 3 A lowers Data0 and Data1
- 4 B lowers Acknowledge

# Asynchronous Pipeline



2 transition latency per stage

18 transition cycle time

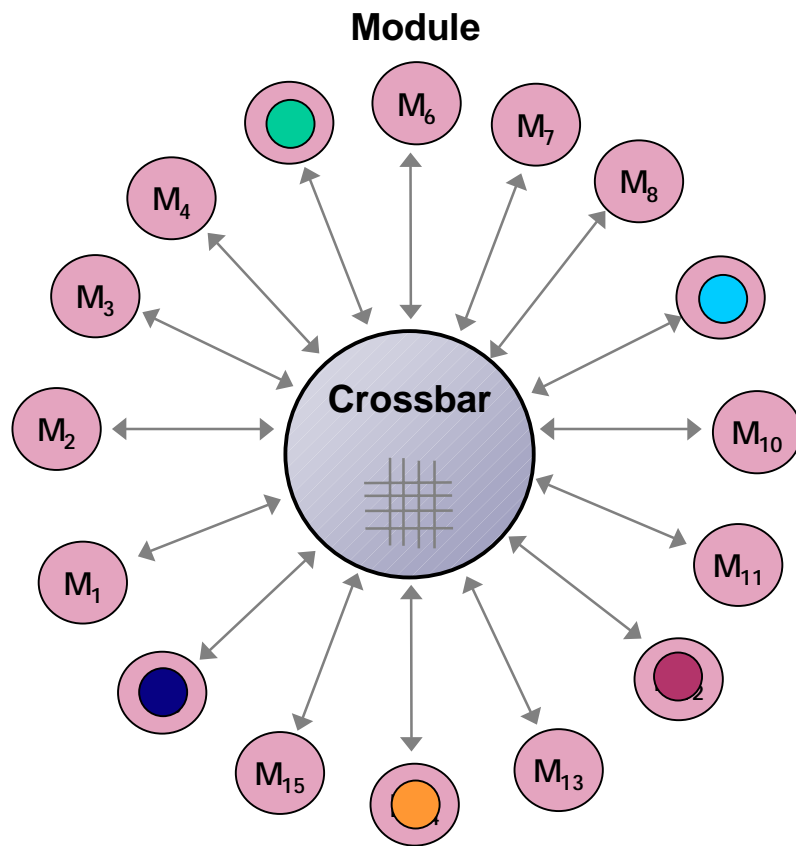
# Fulcrum Asynchronous Advantages

- **High frequency**
- **Low latency**
- **Inherently low power, no wasted transitions (perfect clock gating)**
- **Temperature, voltage, process, delay robustness**
- **Greatly reduced EMI noise**
- **No clock distribution**
- **Built in latches**
- **Fine-grain flow control everywhere**
- **Easy integration of modules at different speeds**

# (Perceived) Disadvantages

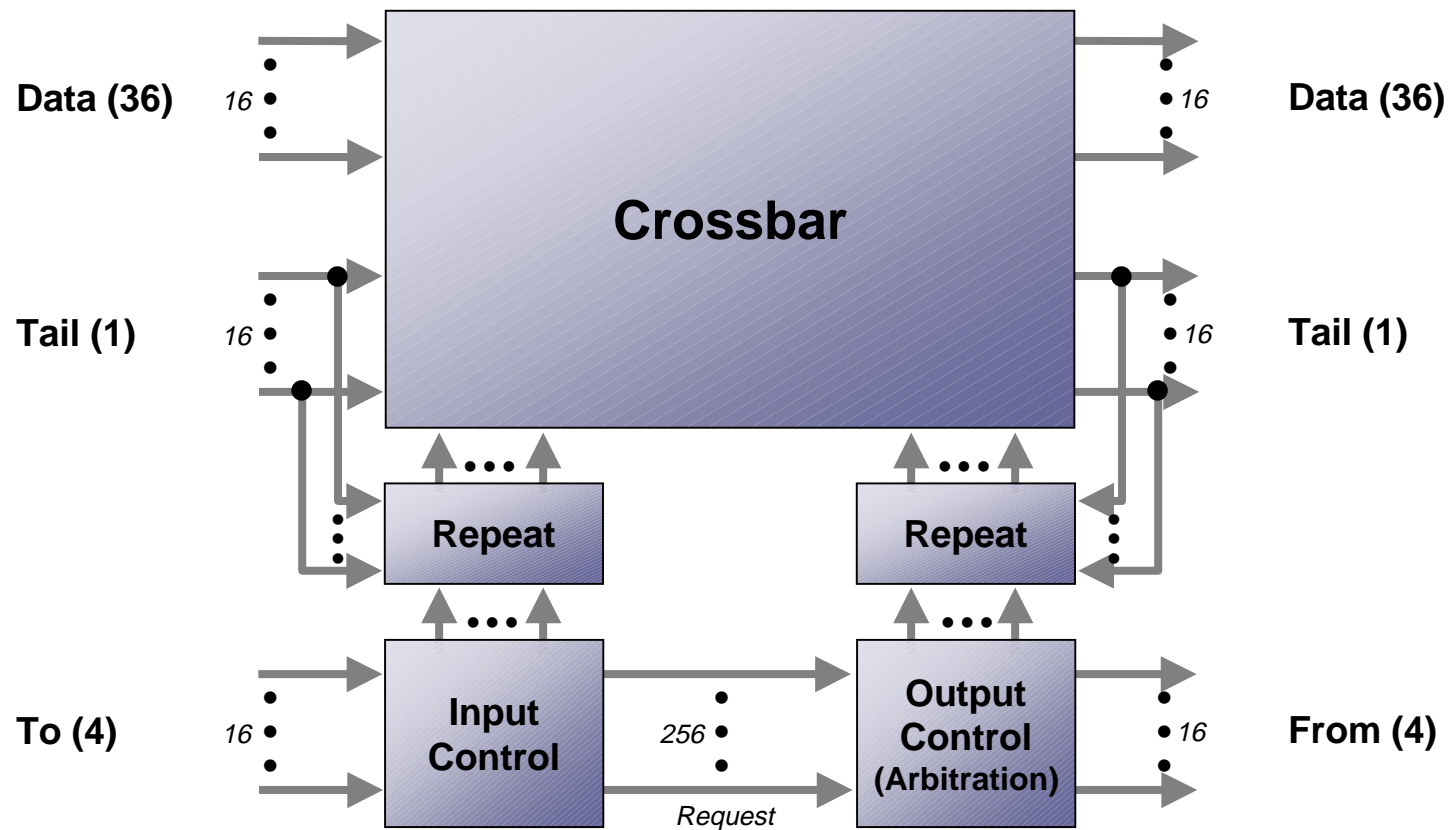
- **Limited commercial tool support**
  - Migrating to commercial tools; partnered with tools providers
- **Additional wires**
  - Feasible in modern fabrication processes
- **Area overhead**
  - Comparable to high-speed synchronous overhead
  - Excellent throughput/area

# SoC Interconnect Functional Overview



- **Crossbar structure**
- **16 full-duplex ports**
  - 36 bits wide
- **> 16 Gbps/port (TSMC 0.18G)**
  - > ½ Tbps aggregate bandwidth
- **Non-blocking architecture**
- **Peer to peer communication**
- **Arbitrary-length bursts**
- **Includes flow control and arbitration**

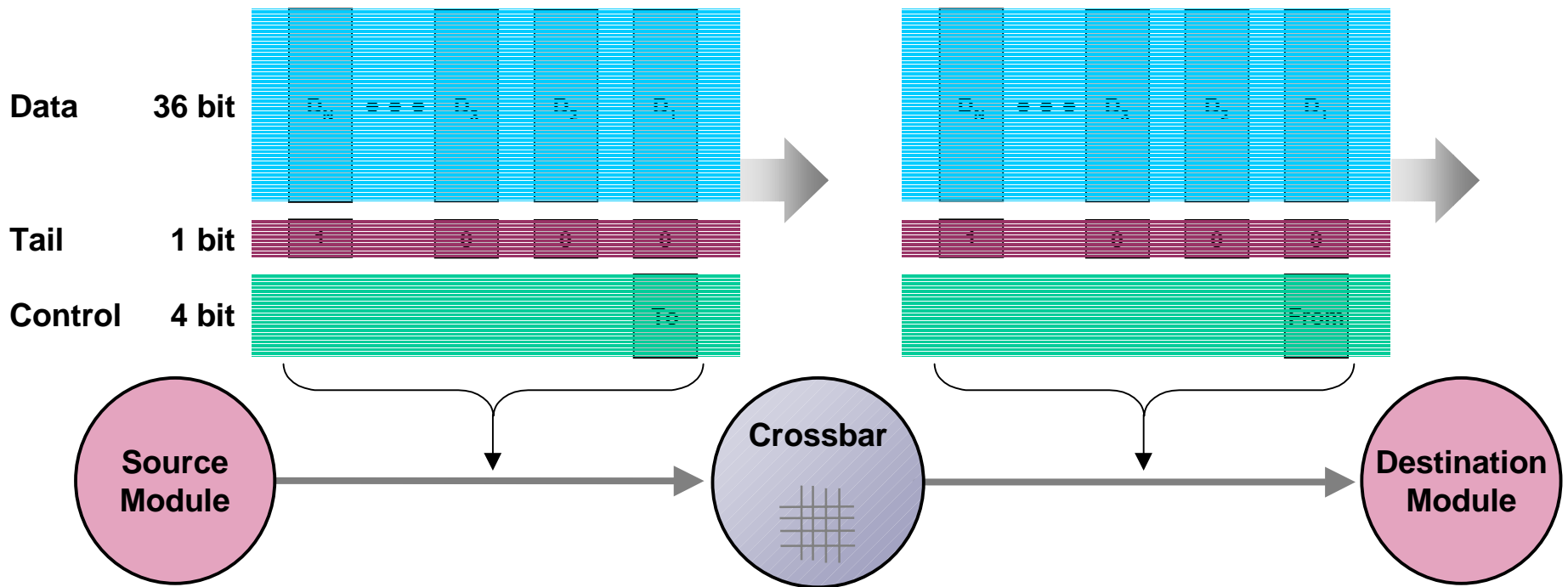
# SoC Interconnect Architecture Overview



# SoC Interconnect Burst Format

Incoming From Source

Outgoing To Destination

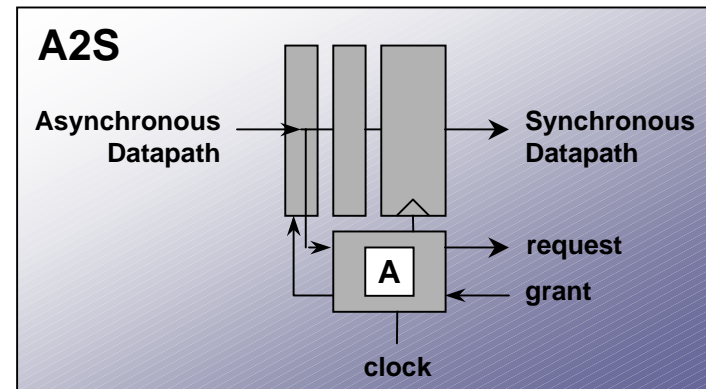
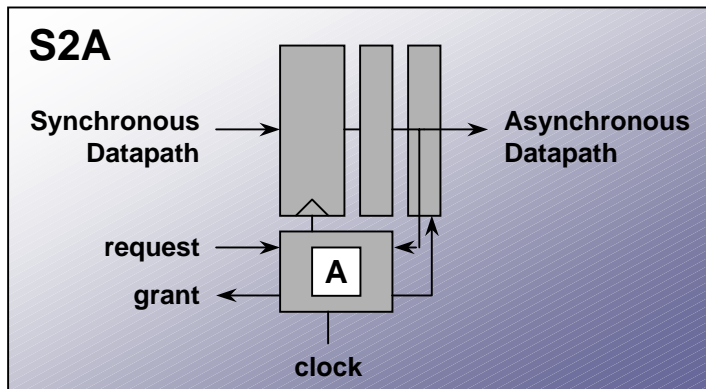


# SoC Interconnect Architectural Features

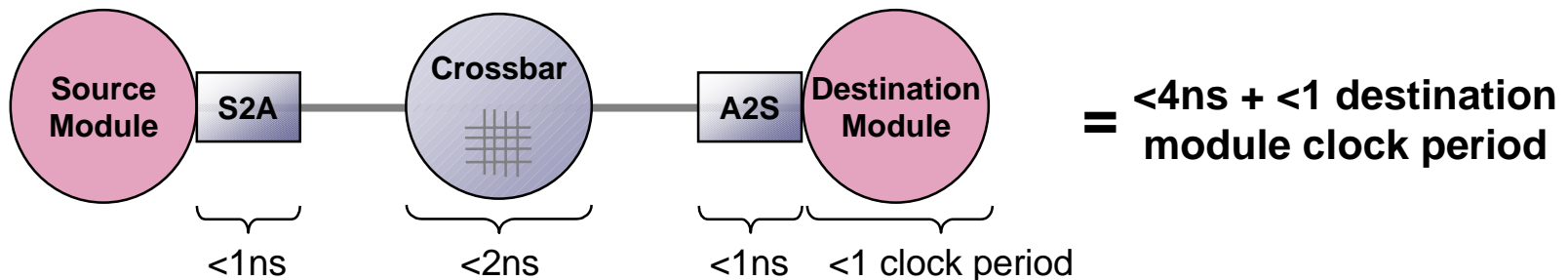
- **Ordering relationships**
  - Bursts from A to B remain ordered
  - Producer/consumer ordering satisfied
  - Split transactions supported
- **Fair arbitration**
  - Work-preserving round robin
  - First come first served in light traffic
  - Bursts transmitted atomically
- **Bus-like behavior**
  - Significantly higher aggregate bandwidth
  - Much less contention

# Synchronous Interfacing

- Channels synchronized with low-latency A2S and S2A converters
  - Synchronous side: request/grant FIFO protocol
  - Asynchronous side: four phase delay-insensitive handshake protocol



- Worst-case latency between two clock domains through crossbar:



# Protocol Examples

- **SoC Load/Store**

- Use first word of burst for address/length header
- Attach N words of data (with error protection) for Store
- Target module sends Load completion back with header and N words of data (with error protection)

- **SoC Send/Interrupt/Signal**

- Message passing, direct memory copies
- In-band signals or interrupts
- In-band cache coherence protocol

- **Switch core**

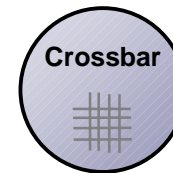
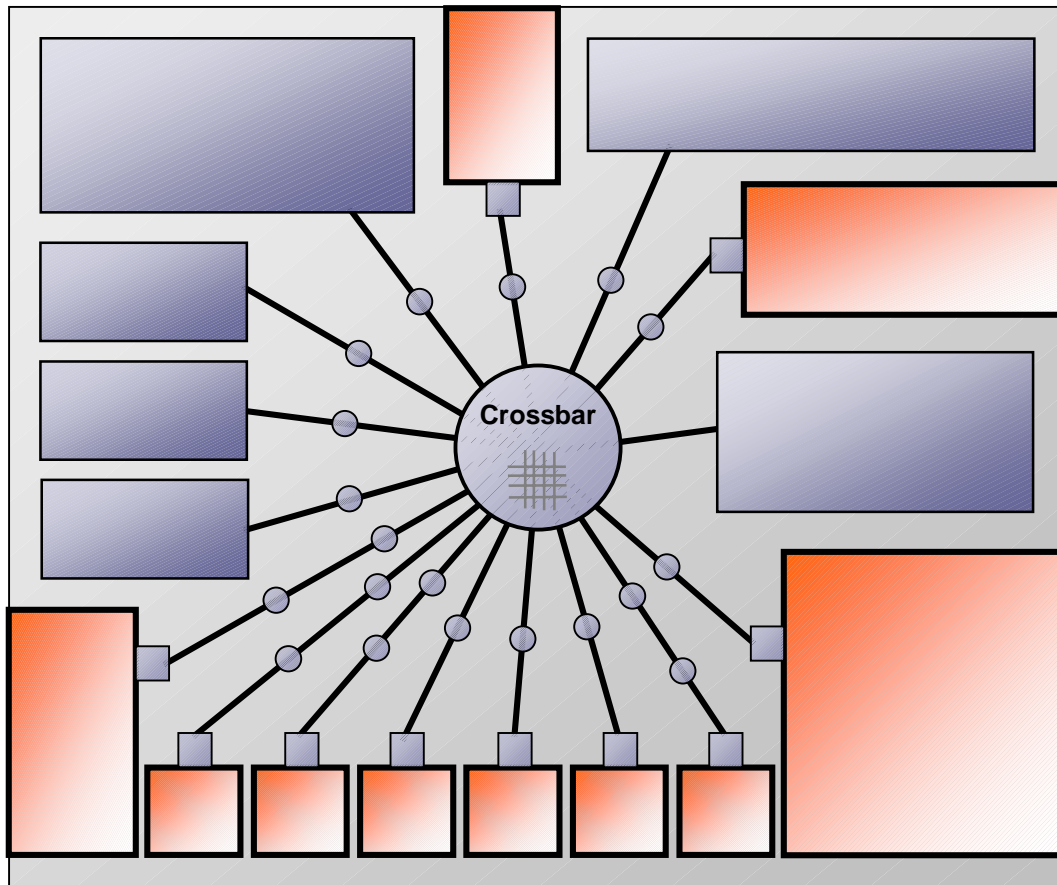
- Derive destination port from header word

- **PCI tunneling**

- 36-bit datapath
- Split transactions
- Bus-style ordering

# SoC Interconnect Generic Application

System on a chip



**-Crossbar:** Includes control & arbitration

○ **-Repeat buffer:** Maintains high throughput; inserted as needed

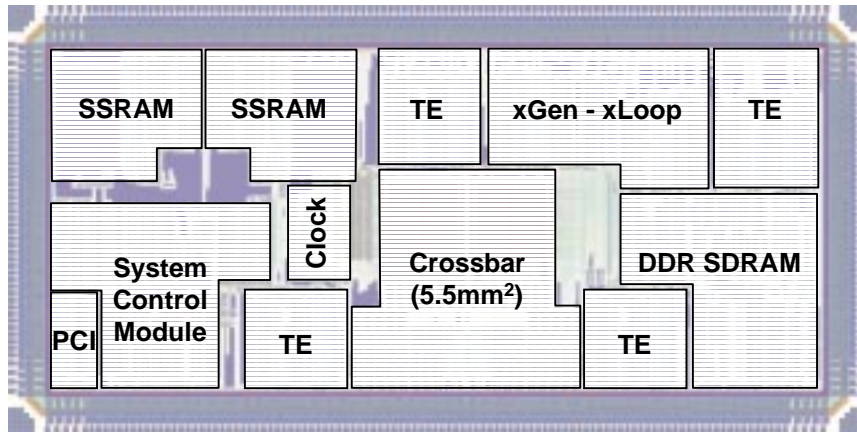
■ **-Sync converter:** Converts to/from a synchronous domain; includes jitter buffer and scan chain

— **-Channel:** Asynchronous channel with built-in flow control

■ **-Asynchronous block**

■ **-Synchronous block**

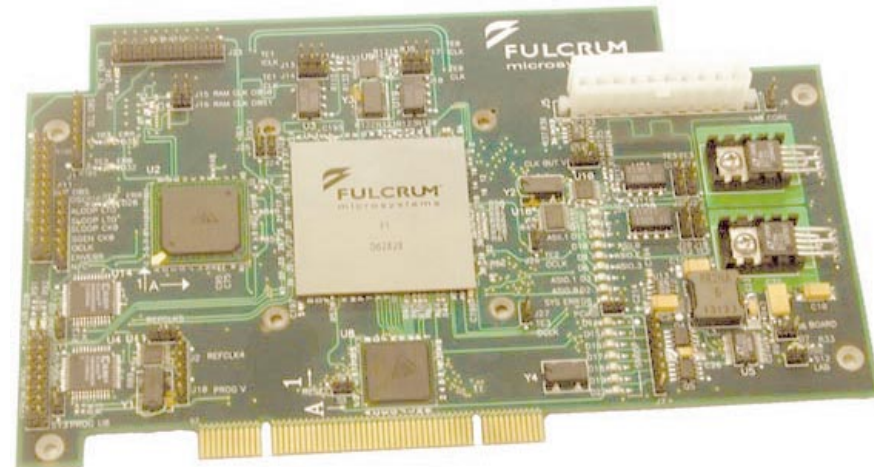
# F1 Project



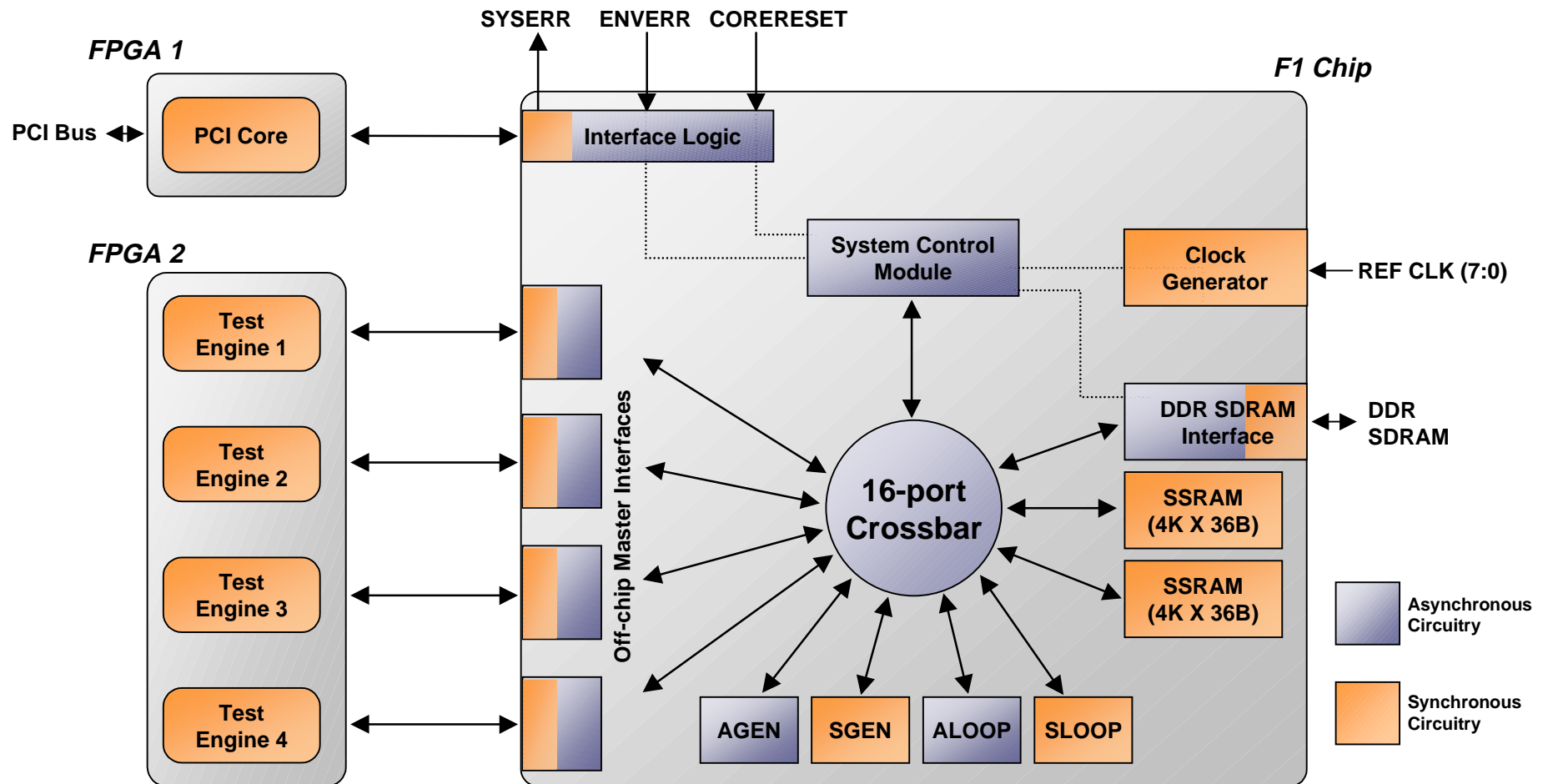
- 5 man years
- 450MHz (TSMC 0.18 G)
- 5.5 M transistors
- 200 unique leaf cells
- 50mm<sup>2</sup>
- Crossbar: 5.5mm<sup>2</sup>

## System Elements:

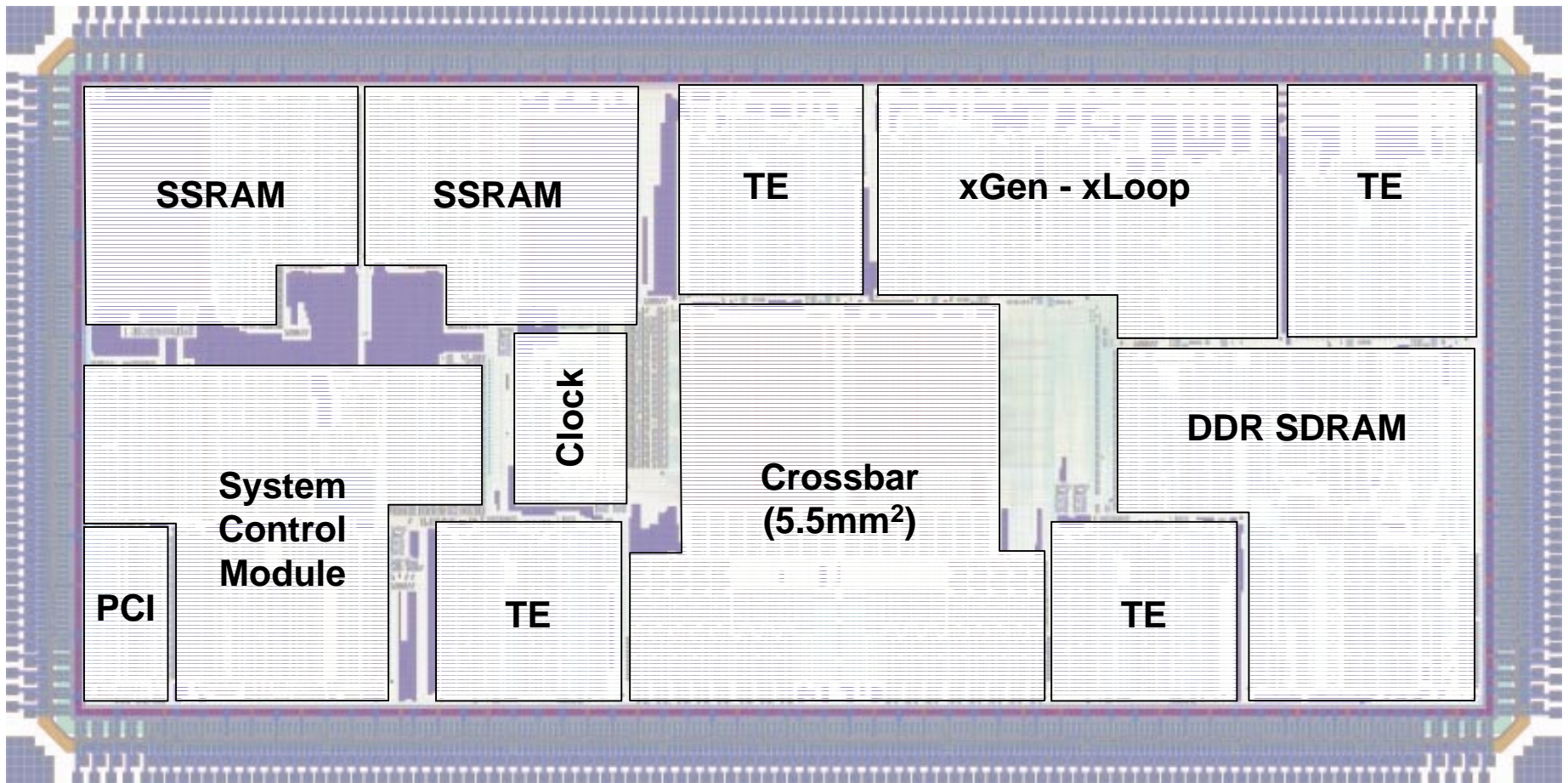
- SoC Interconnect (16-port crossbar)
  - >16 Gbps/port, full duplex
  - > ½ Tbps aggregate bandwidth
- DDR SDRAM controller
- Test engine interfaces
- PCI controller interface



# F1 Board Block Diagram

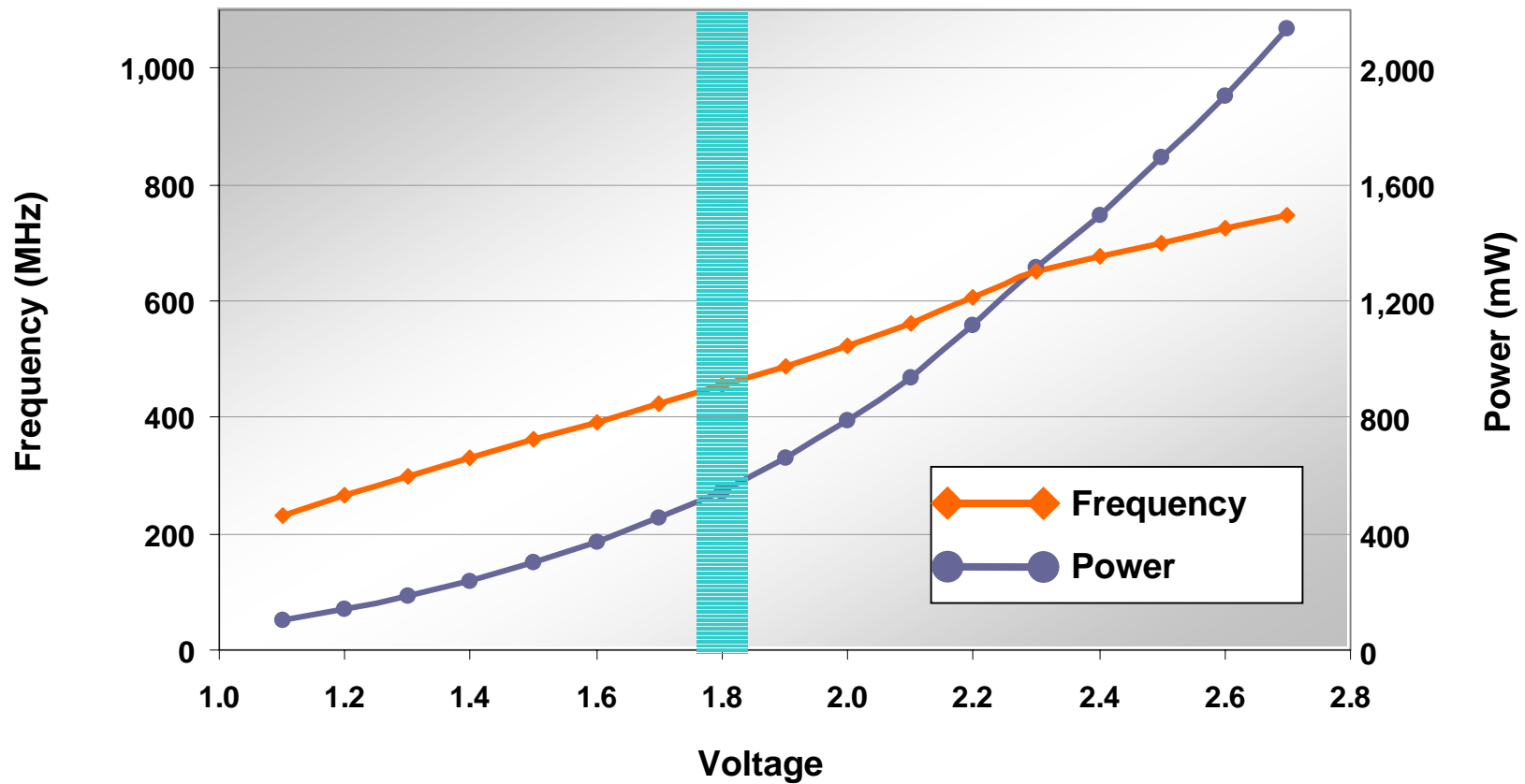


# F1 Chip



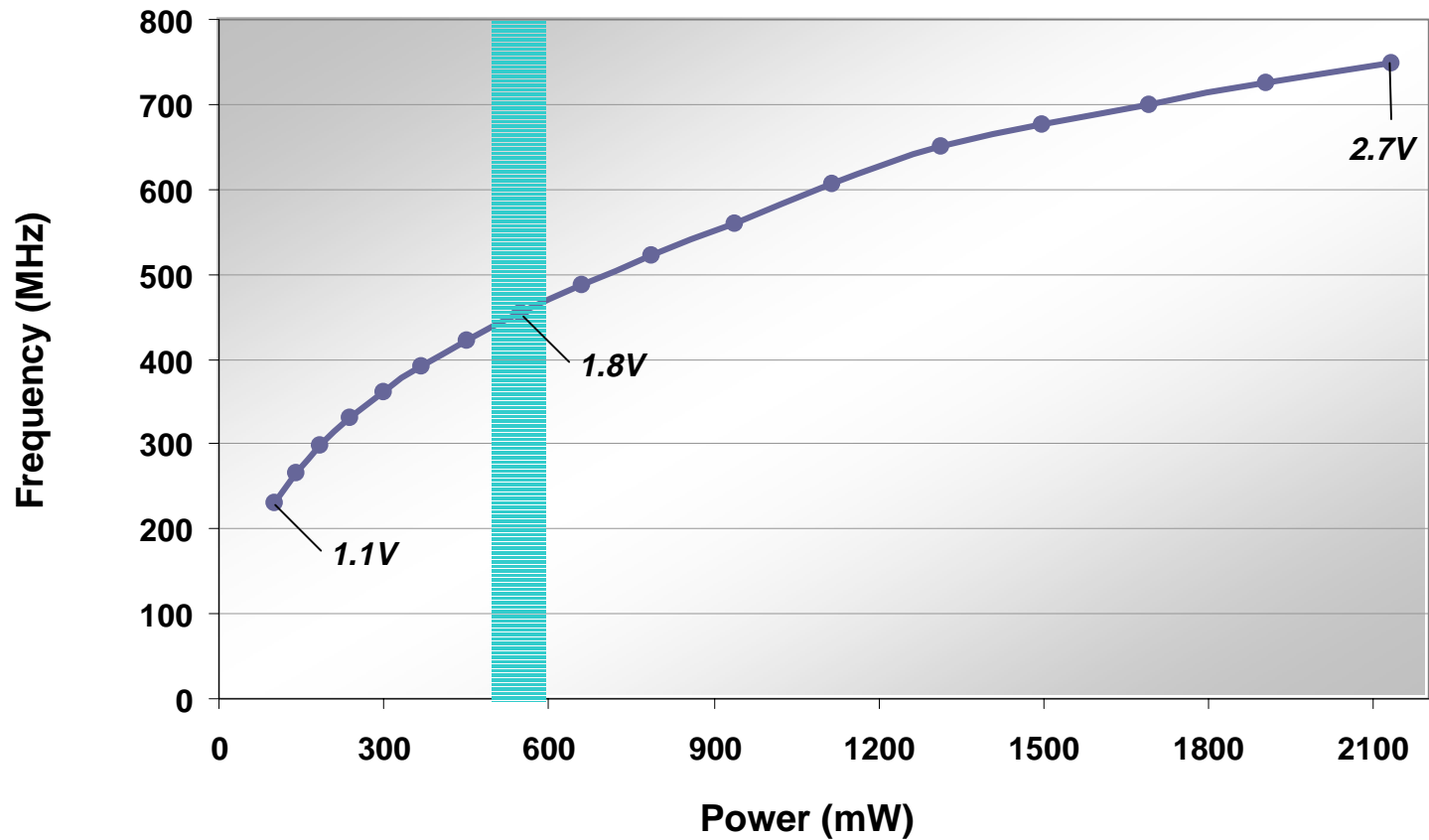
# F1 Frequency and Power vs. Voltage

*One-way Burst Transfer (per link)*



# F1 Frequency vs. Power

*One-way Burst Transfer (per link)*



# Summary Analysis (TSMC 0.18 G)

- **High throughput**
  - >16 Gbps/port, full duplex (>1/2 Tbps aggregate bandwidth)
- **Very high burst rate**
  - 225M bursts/second/port (3.6B aggregate bursts/second)
- **Very low latency**
  - Crossbar latency: <2ns
  - Module-to-module latency: <4ns + <1 destination module clock period
- **Modest power profile**
  - Scales linearly with usage (no standby power)
  - 4W max at 260 Gbps transfer rate (much less in typical operation)
- **Small footprint**
  - 5.5mm<sup>2</sup> (and shrinking)

# Thank You!

**Andrew Lines**

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“A group of engineers wants to turn the microprocessor world on its head by doing the unthinkable: tossing out the clock and letting the signals move about unencumbered. For those designers, inspired by research conducted at Caltech, **clocks are for wimps.**”

*Times, May 28, 2002*