

Sub-lithographic Semiconductor Computing Systems

André DeHon

andre@cs.caltech.edu

In collaboration with
Charles Lieber, Patrick Lincoln,
and John Savage



Approaching the Bottom

- In 1959, Feynman pointed out we had
 - “plenty of room at the bottom”
- Suggested:
 - wires ~ 10-100 atoms diameter
 - circuits ~ few thousands angstroms
~ few hundred nm

Approaching the Bottom

- Today we have 90nm Si processes
 - bottom is not so far away
- Si Atom
 - 0.5nm lattice spacing
 - 90nm ~ 180 atoms diameter wire

Exciting Advances in Science

- Beginning to be able to manipulate things at the “bottom” -- atomic scale engineering
 - designer/synthetic molecules
 - carbon nanotubes
 - silicon nanowires
 - self-assembled mono layers
 - designer DNA

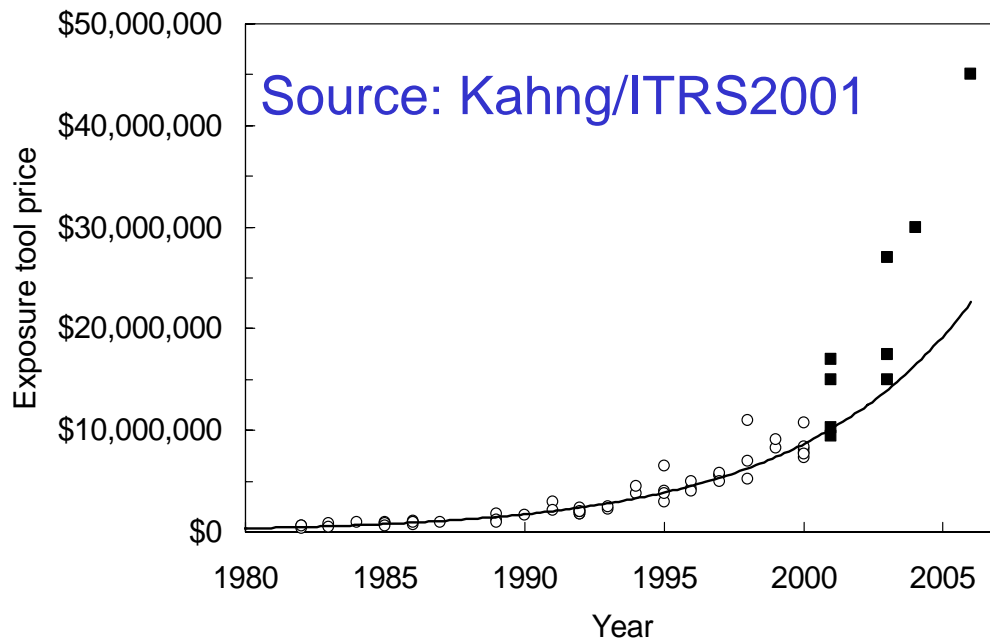
Question

- Can we build interesting computing systems without lithographic patterning?
- **Primary interest:**
below lithographic limits

Why do we care?

- Lithographic limitations
 - Already stressing PSM
 - ...xrays, electron projection...

- Lithographic costs



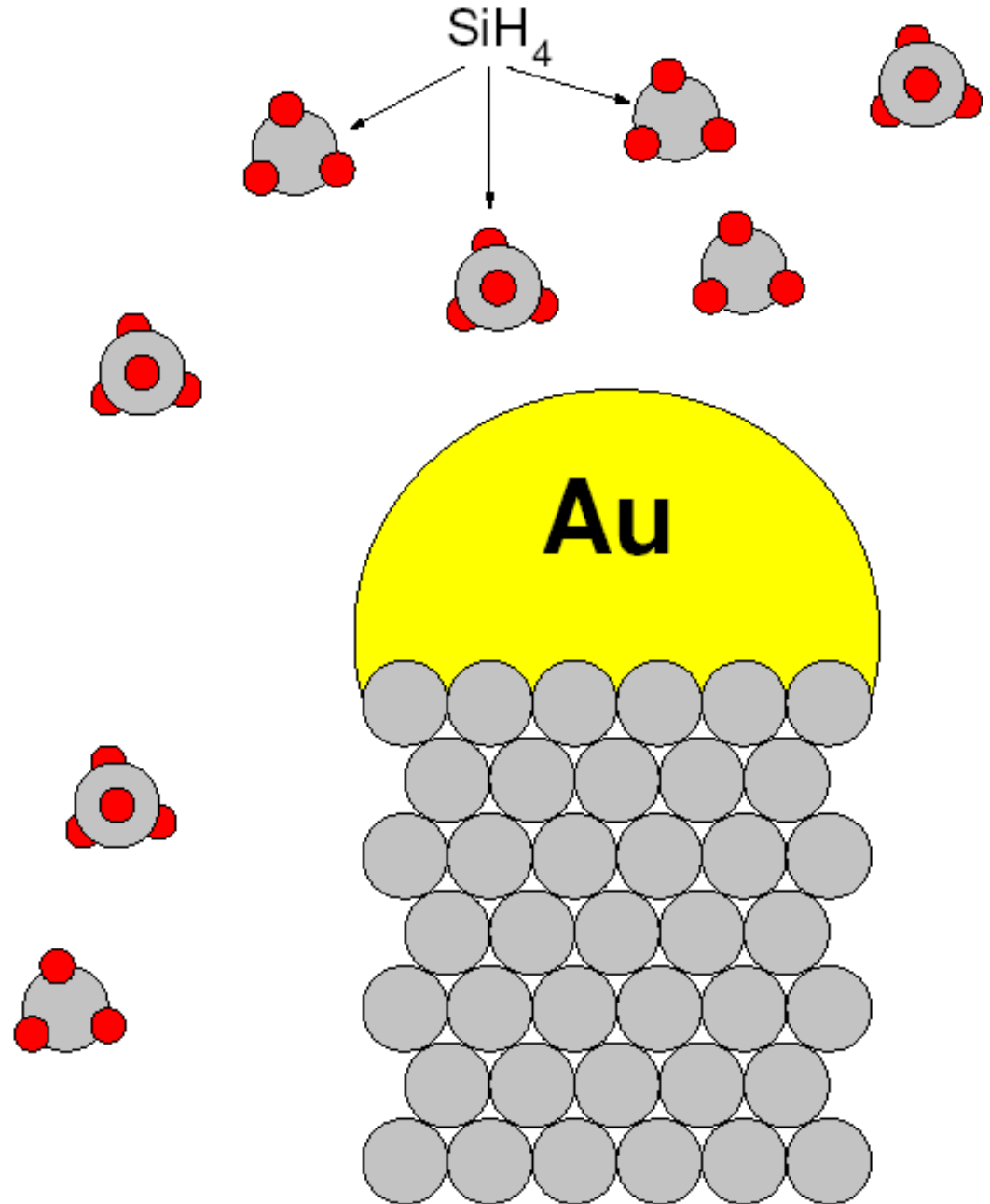
Today's Talk

Bottom up tour: from Si atoms to Computing

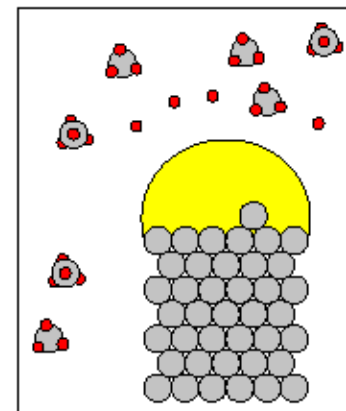
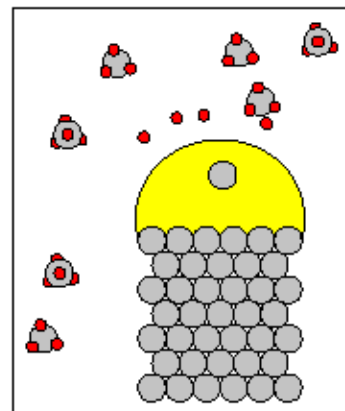
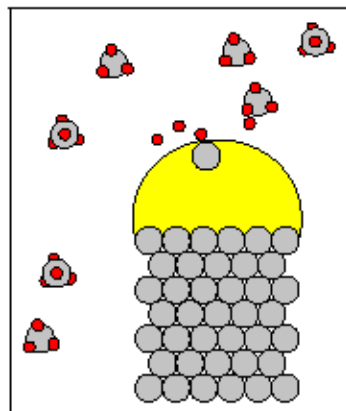
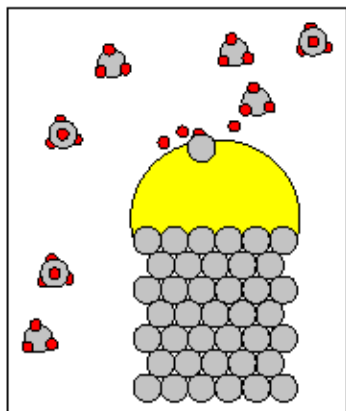
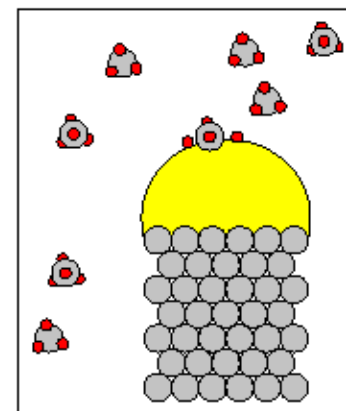
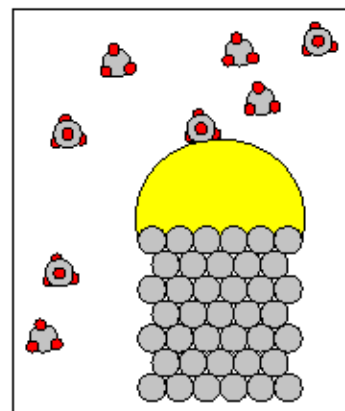
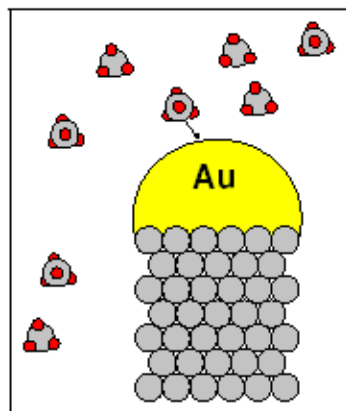
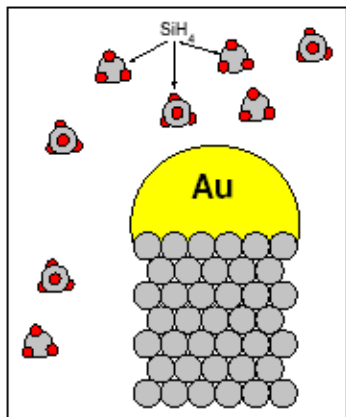
- Nanowire growth
- Nanowire devices
- Nanowire assembly
- Nanowire differentiation
- Nanowire coding
- Nanoscale memories from nanowires
- Nanoscale PLAs
- Defect tolerance
- Universal Computing blocks defined at nanoscale

SiNW Growth

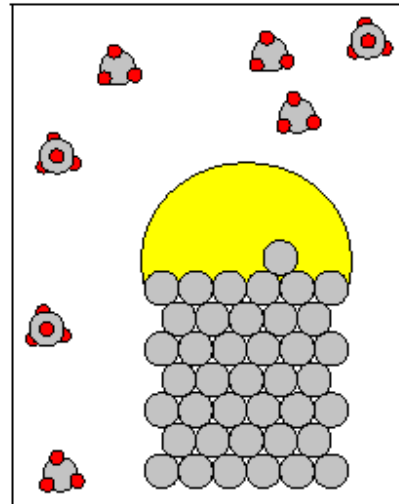
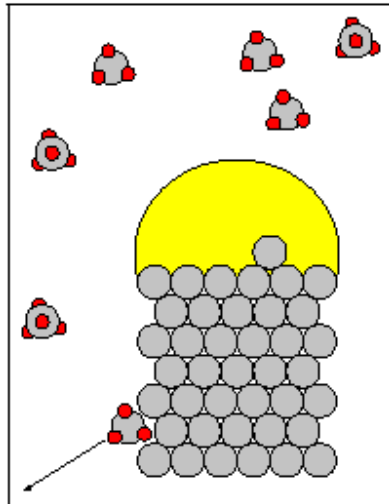
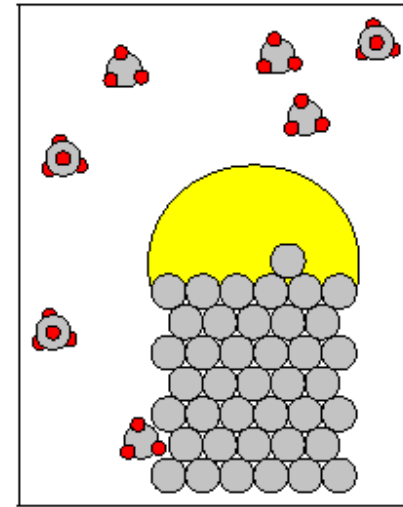
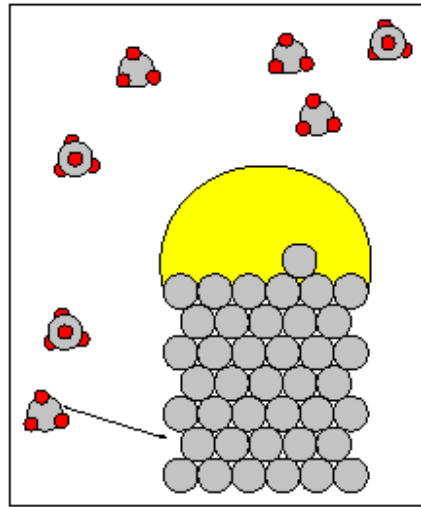
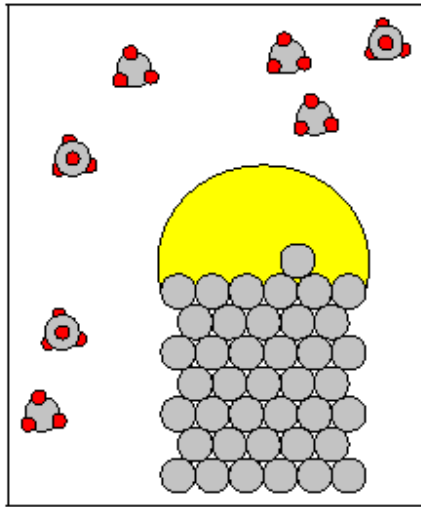
- Atomic structure determines feature size
- Self-same crystal structure constrains growth
- Catalyst defines/constrains structure



SiNW Growth



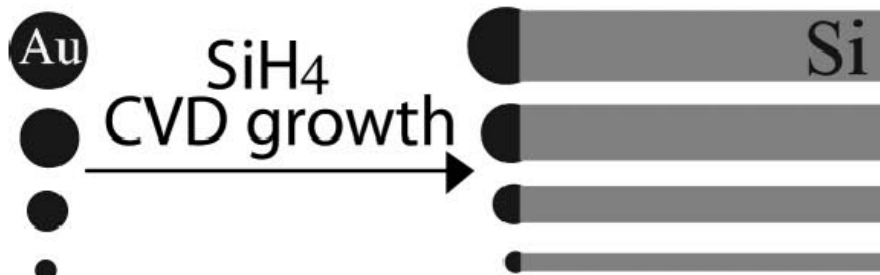
SiNW Growth



Building Blocks

Semiconducting Nanowires

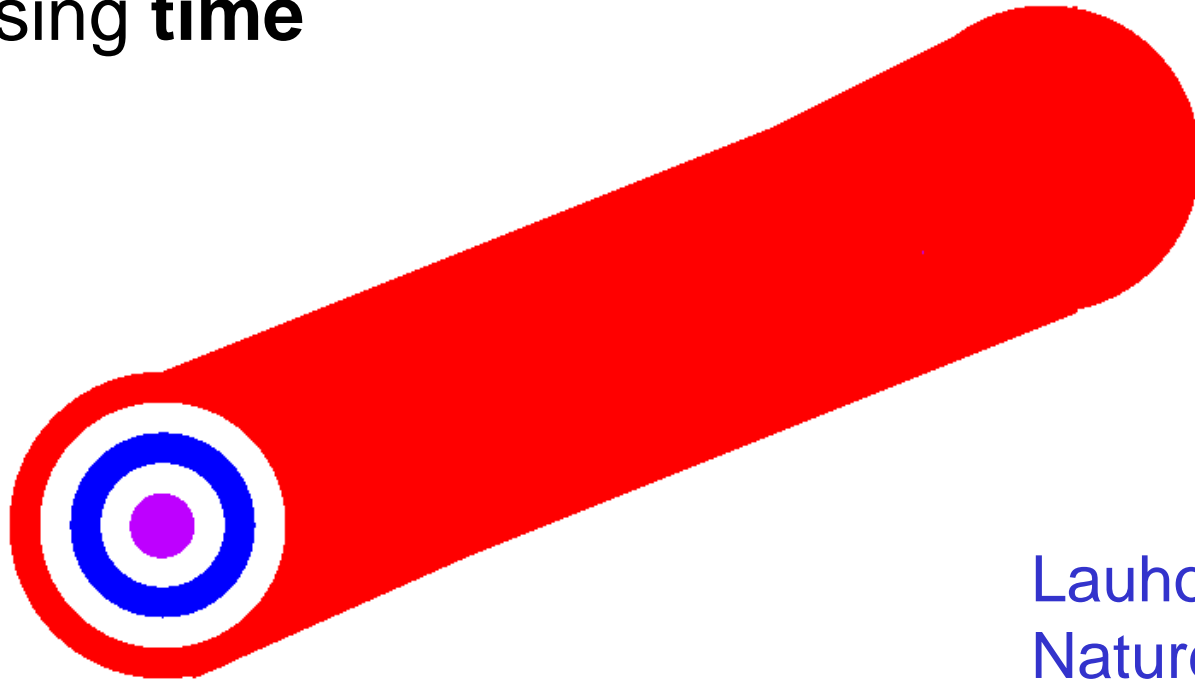
- Few nm's in diameter (*e.g.* 3nm)
 - Diameter controlled by seed catalyst
- Can be microns long
- Control electrical properties via doping
 - Materials in environment during growth
 - Control thresholds for conduction



From:
Cui...Lieber
APL v78n15p2214

Radial Modulation Doping

- Can also control doping profile radially
 - To atomic precision
 - Using **time**

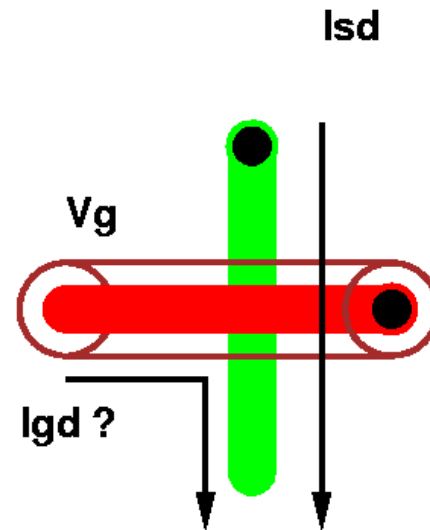
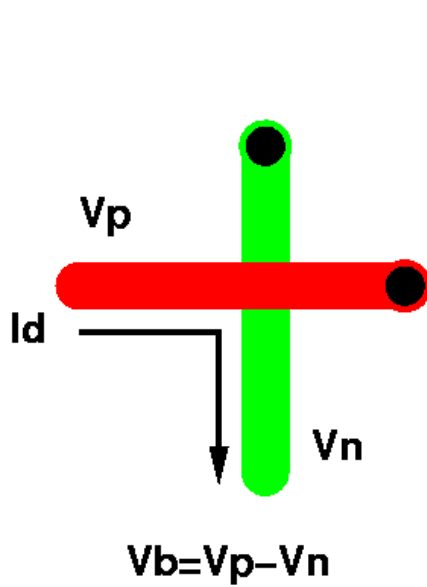


Lauhon et. al.
Nature 420 p57

Devices

Doped nanowires give:

Diode and FET Junctions

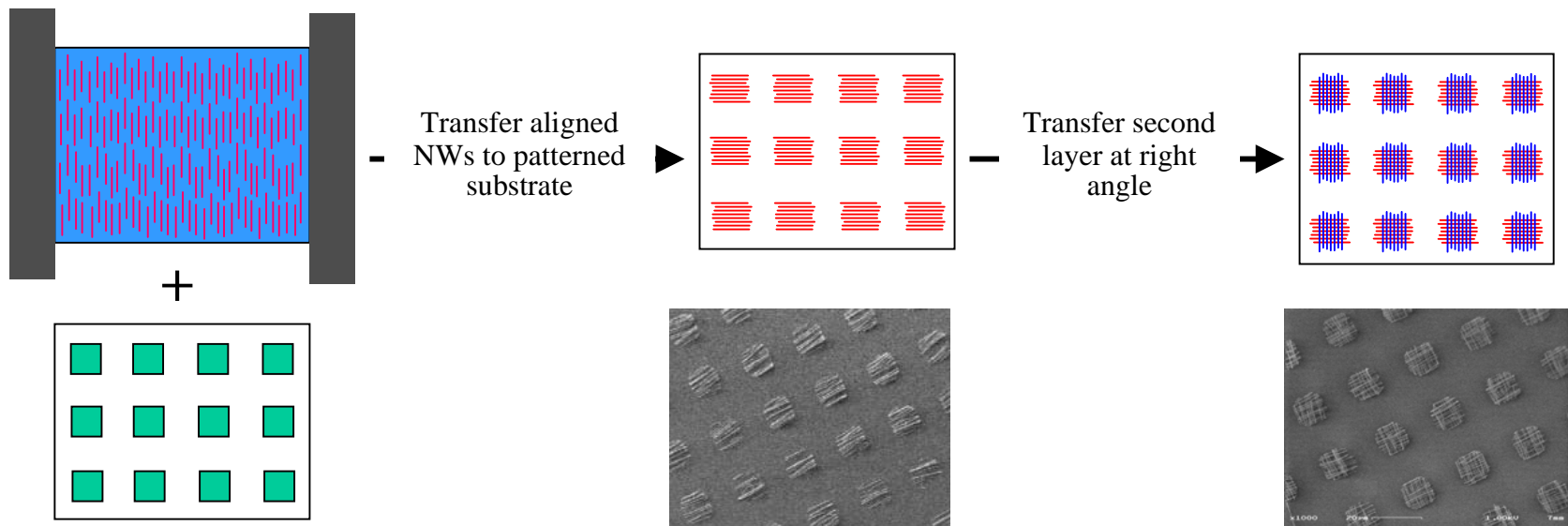


Cui...Lieber
Science 291 p851

Huang...Lieber
Science 294 p1313

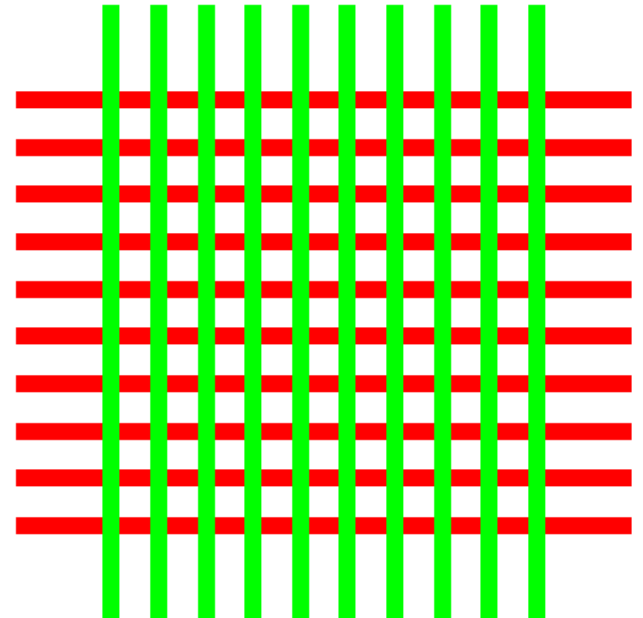
Langmuir-Blodgett (LB) transfer

- Can transfer tight-packed, aligned SiNWs onto surface
 - Maybe grow sacrificial outer radius, close pack, and etch away to control spacing



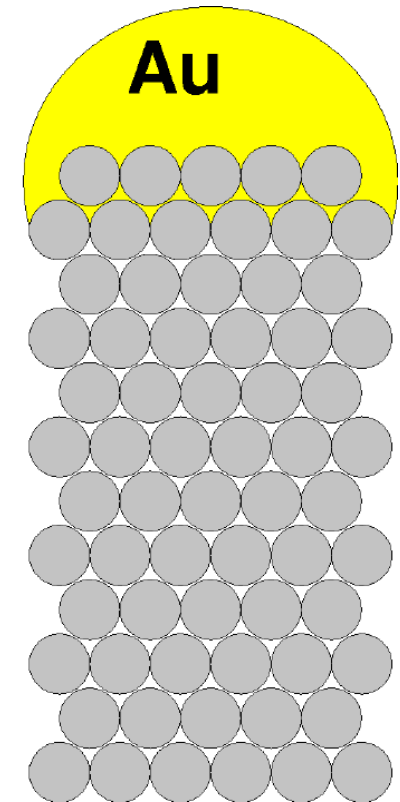
Homogeneous Crossbar

- Gives us homogeneous NW crossbar
 - Undifferentiated wires
 - All do the same thing



Control NW Dopant

- Can define a dopant profile along the length of a wire
 - Control lengths by **timed** growth
 - Change impurities present in the environment as a function of time



Gudiksen et. al.
Nature 415 p617

Björk et. al.
Nanoletters 2 p87

Control NW Dopant

- Can define a dopant profile along the length of a wire
 - Control lengths by **timed** growth
 - Change impurities present in the environment as a function of time
- Get a SiNW banded with differentiated conduction/gate-able regions



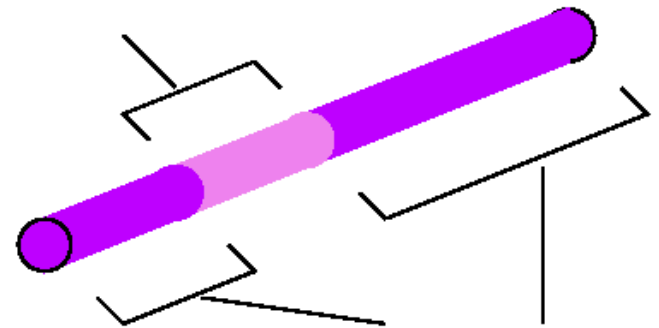
Gudskien et. al.
Nature 415 p617

Björk et. al.
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Enables: Differentiated Wires

- Can control which regions of a wire are gate-able
 - Lightly doped regions \rightarrow gate with low threshold
 - Heavily doped regions \rightarrow gate with high threshold
- Can engineer so portions of wire oblivious to applied voltage (always conduct) and others controlled

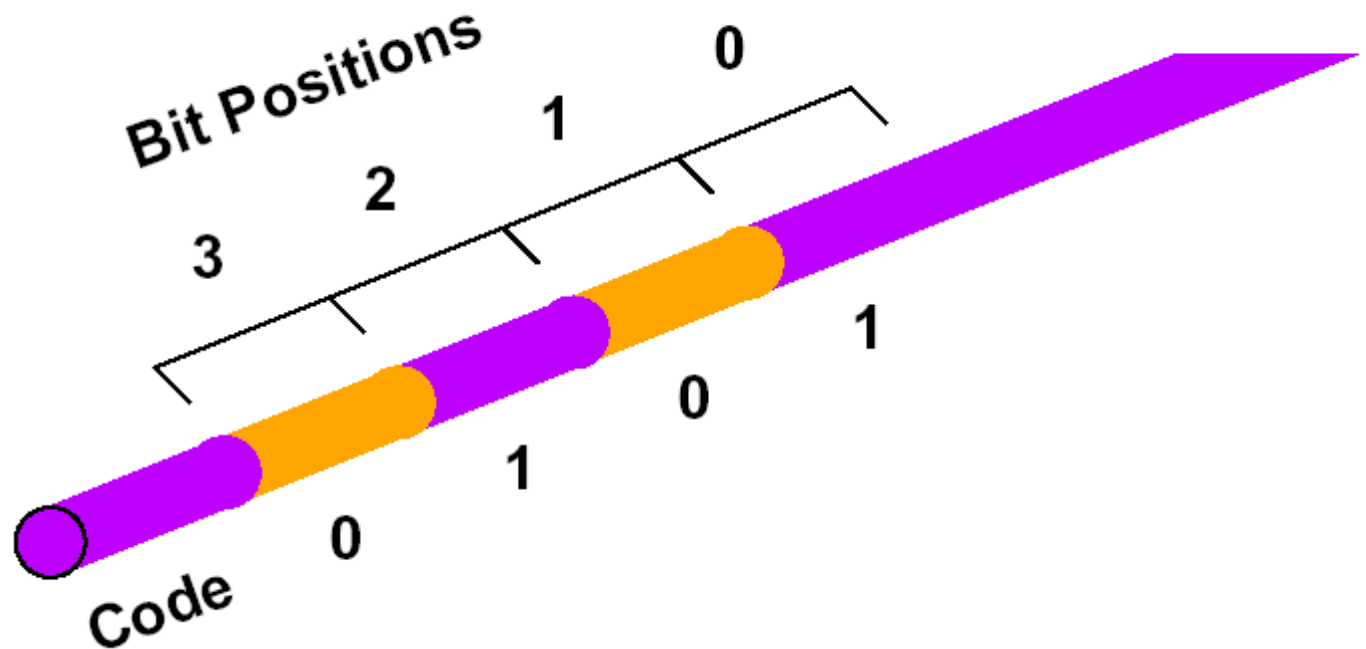
**Conduct only
with field $< 1\text{ V}$**



Conduct any field $< 5\text{V}$

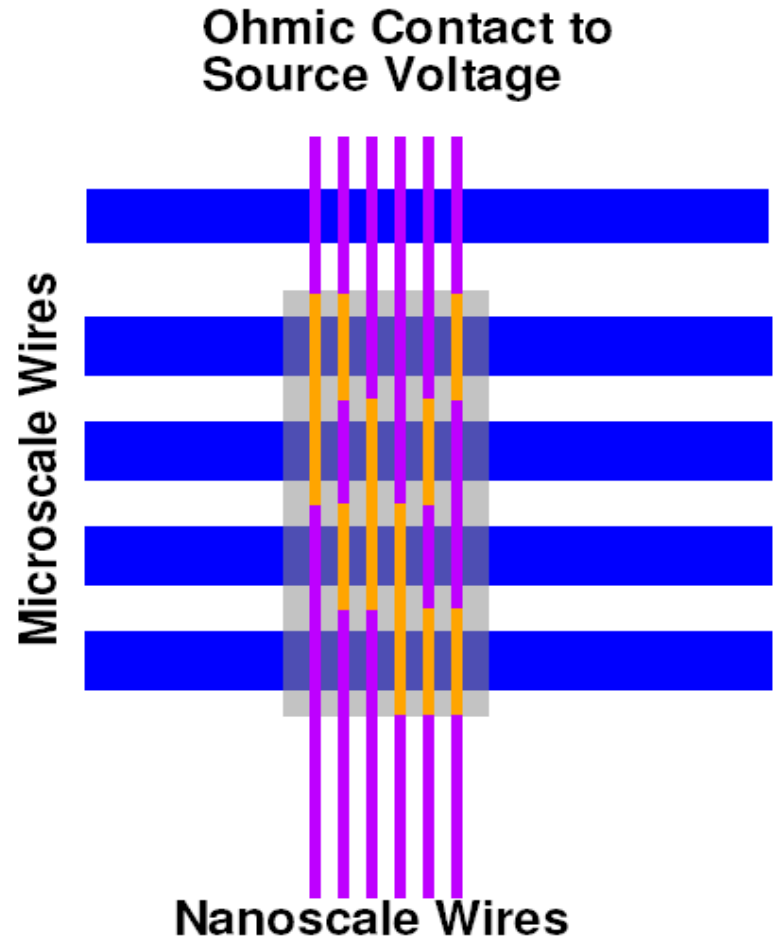
Coded Wires

- By selectively making bit-regions on wires either highly or lightly doped
 - Can give the wire an address



Unique Set of Codes

- **If** we can assemble a set of wires with unique codes
 - We have an address decoder
 - Apply a code
 - k-hot code
 - Unique code selects a single wire

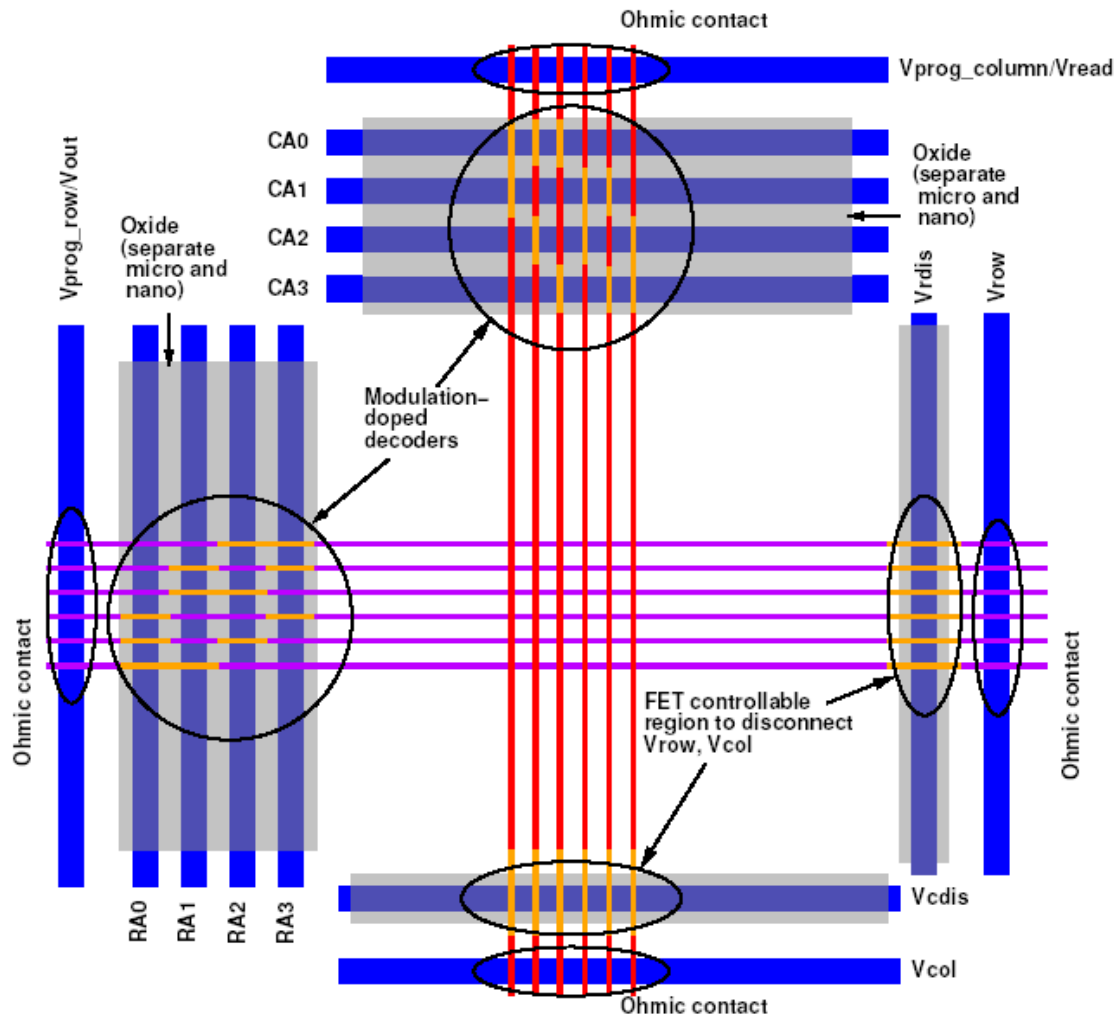


Statistical Coding

- Unique Code set achievable with statistical assembly (random mixing)
- Consider:
 - Large code space (10^6 codes)
 - Large number of wires of each type (10^{12})
 - Small array (10 wires) chosen at random
- Likelihood all 10 unique?
 - Very high! (99.995%)

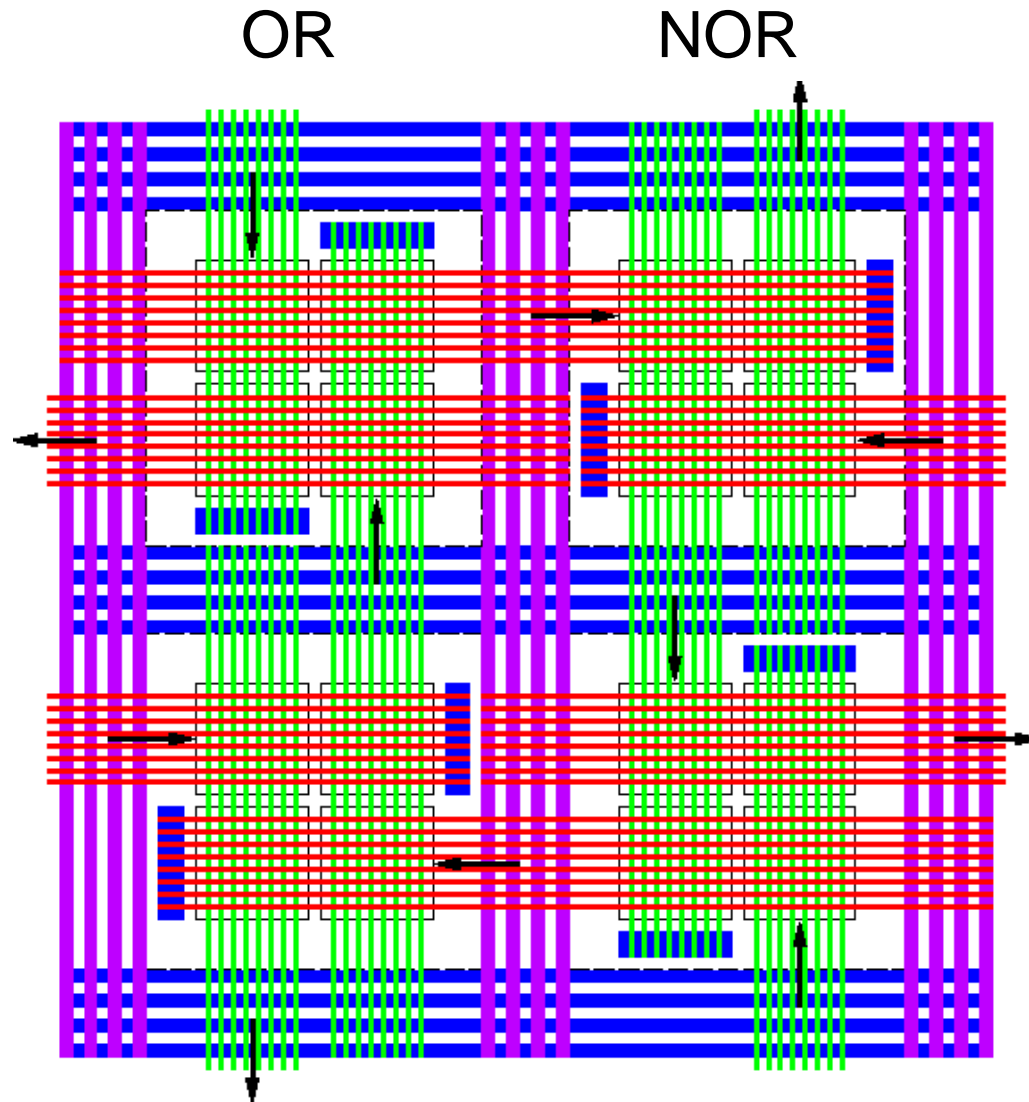
DeHon et. al.
IEEE TNANO to appear

Basis for Sublithographic Memory

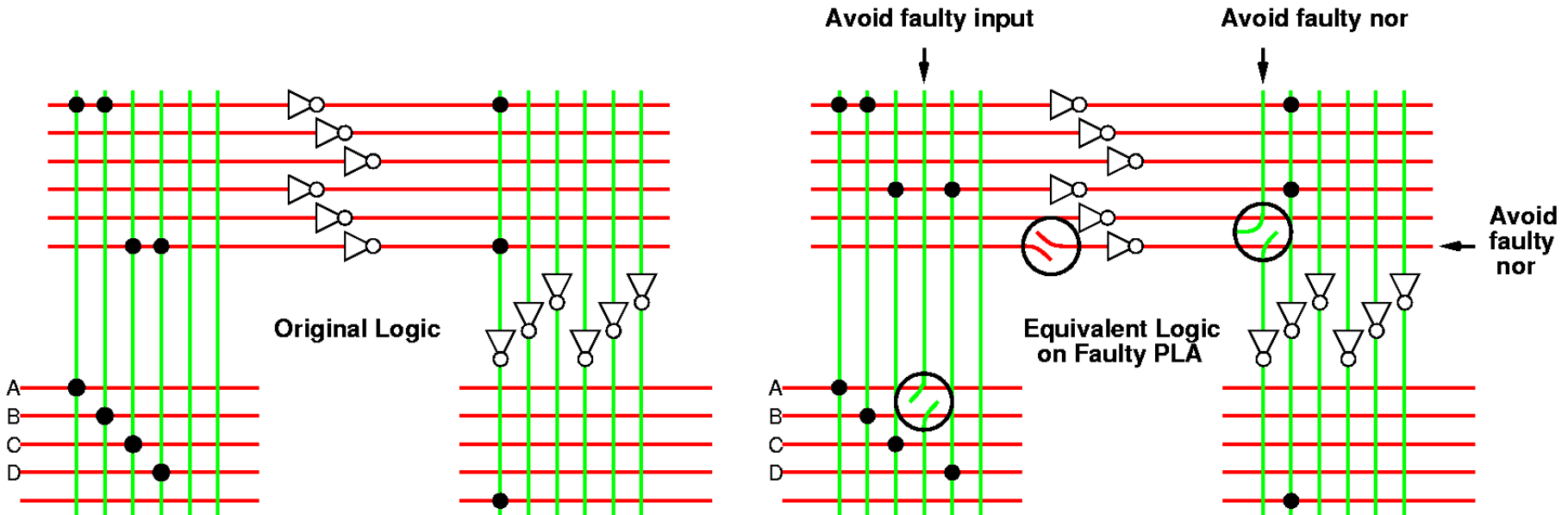


Connected PLAs

- Programmable OR planes like memory
- NW cross arrays for interconnect
- FET planes to restore/invert
- Manhattan routing
- Fully nanoscale computing



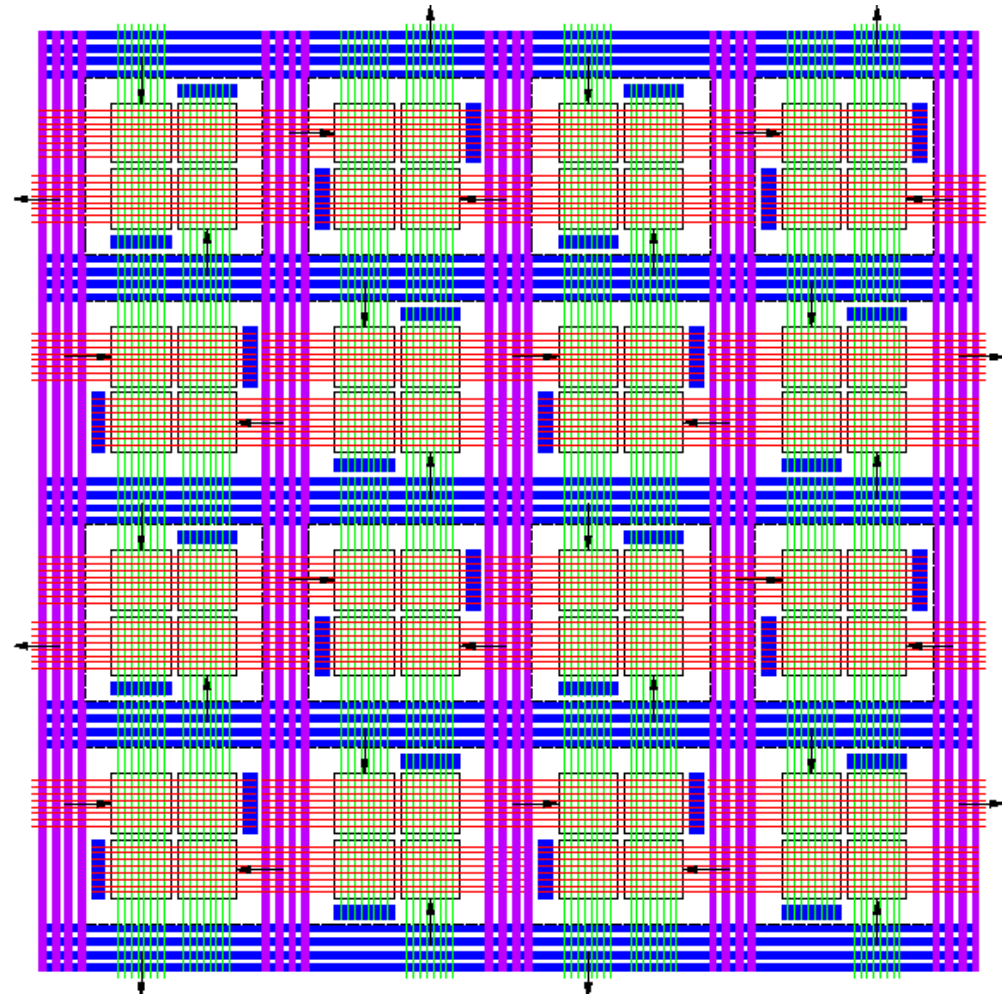
Defect Tolerant



All components (PLA, routing, memory) interchangeable;
Allows local programming around faults

Universal Computing Device

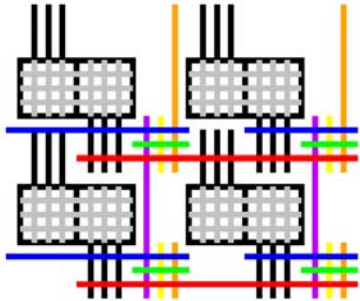
- Tile Array Block
- Programmable Array
- NOR universal
- Implement any computation



DeHon
IEEE TNANO v2n1

Construction Review

- Seeding control NW diameter
- Timed growth controls doping profile along NW
- LB flow to assemble into arrays
- Timed etches to separate/expose features
- Assemble on lithographic scaffolding
- Stochastic construction of address coding allow micro→nanoscale addressing
- Differentiate at nanoscale via post-fabrication programming
- All compatible with conventional semiconductor processing
 - Key feature is decorated nanowires

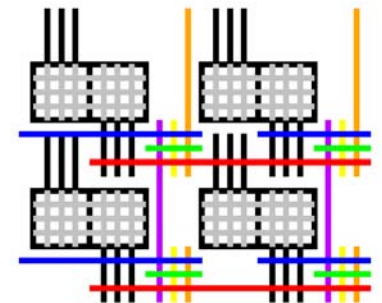


Summary

- Can engineer designer structures at atomic scale
- Must build regular structure
 - Amenable to self-assembly
- Can differentiate
 - Stochastically
 - Post-fabrication programming
- Sufficient for Memories and Universal, Programmable Architecture
- Sufficient building blocks to define computing systems without lithography

Additional Information

- <<http://www.cs.caltech.edu/research/ic/>>
- <<http://www.cmliris.harvard.edu/>>

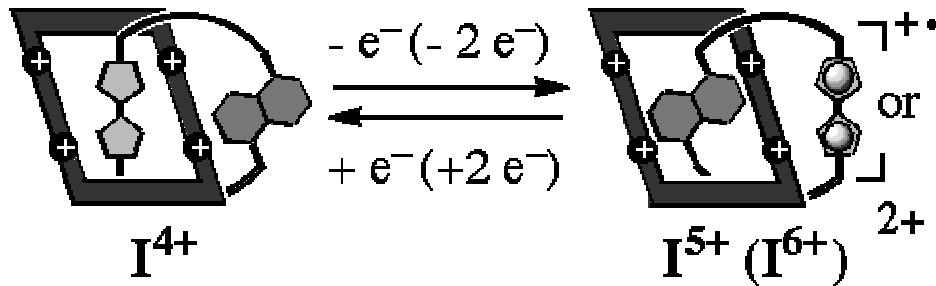
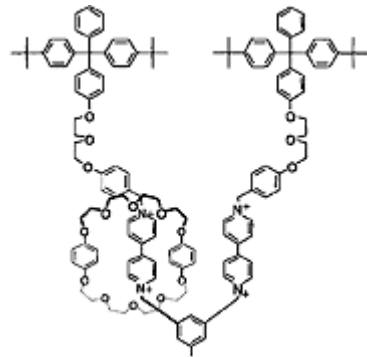


Additional Slides

- Memory Elements
- Logic
- Code Size
- Array Size

Switches / Memories

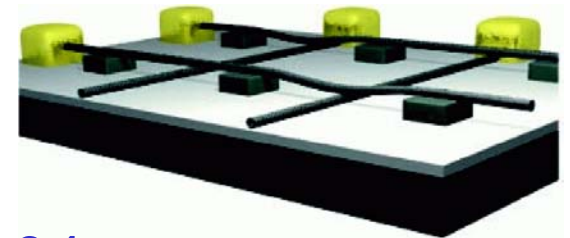
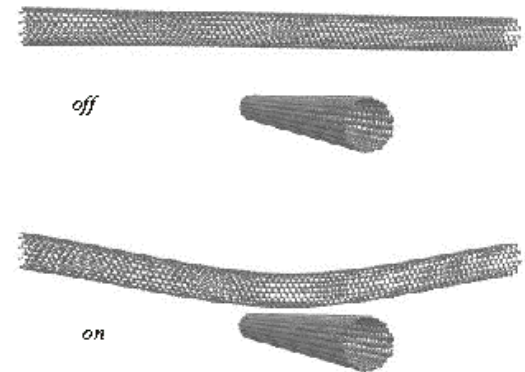
Molecular Switches



Collier et. al.
Science 289 p1172

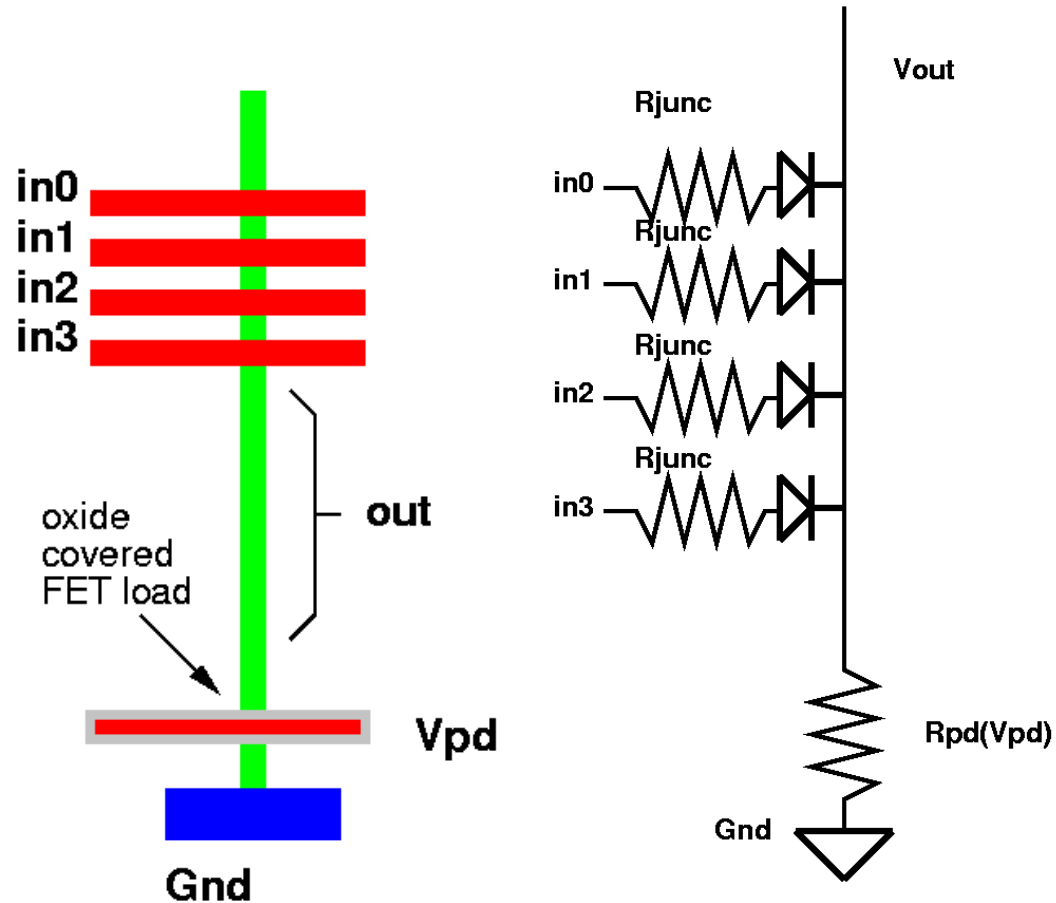
Ruekes et. al.
Science 289 p04

Electrostatic Switches



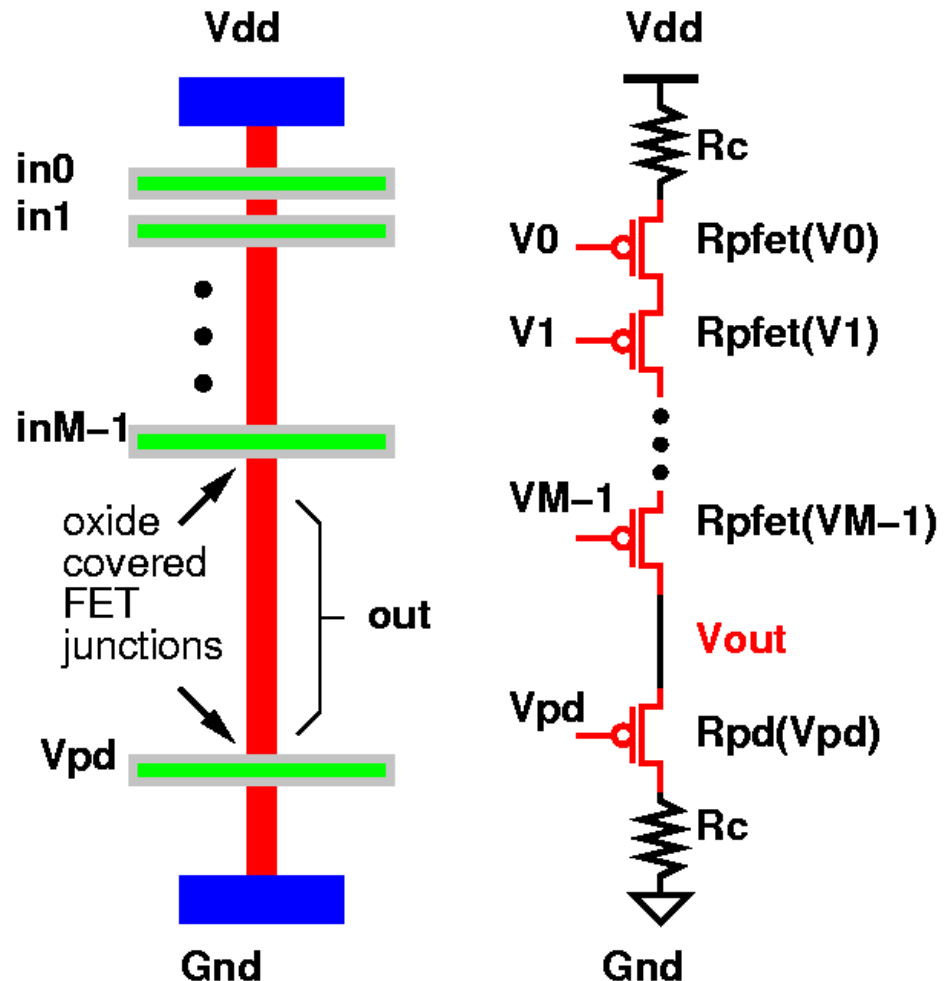
Diode Logic

- Arise directly from touching NW/NTs
- Passive logic
- Non-restoring
- Non-volatile Programmable crosspoints

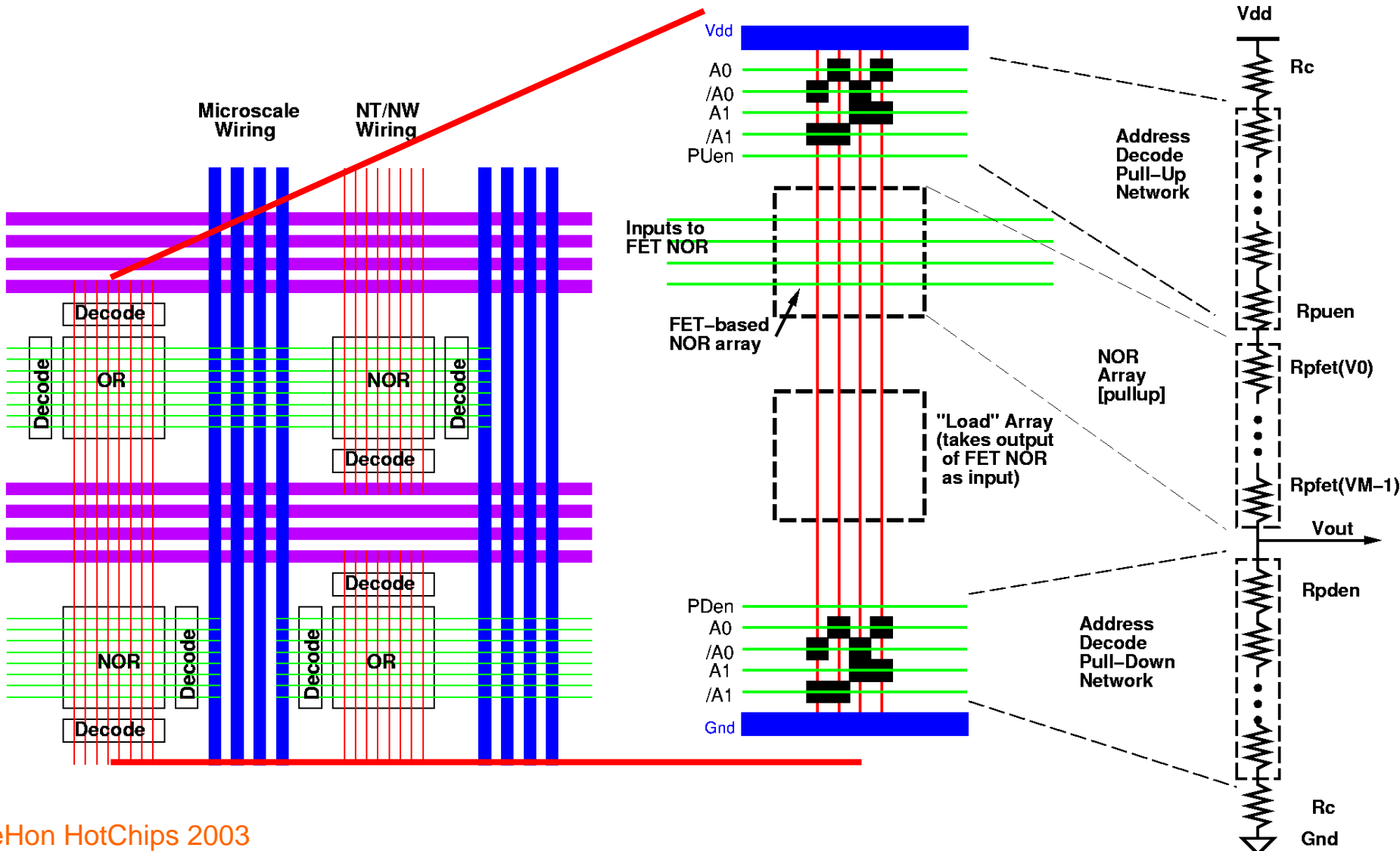


PMOS-like Restoring FET Logic

- Use FET connections to build **restoring** gates
- Static load
 - Like NMOS (PMOS)
- Maybe precharge

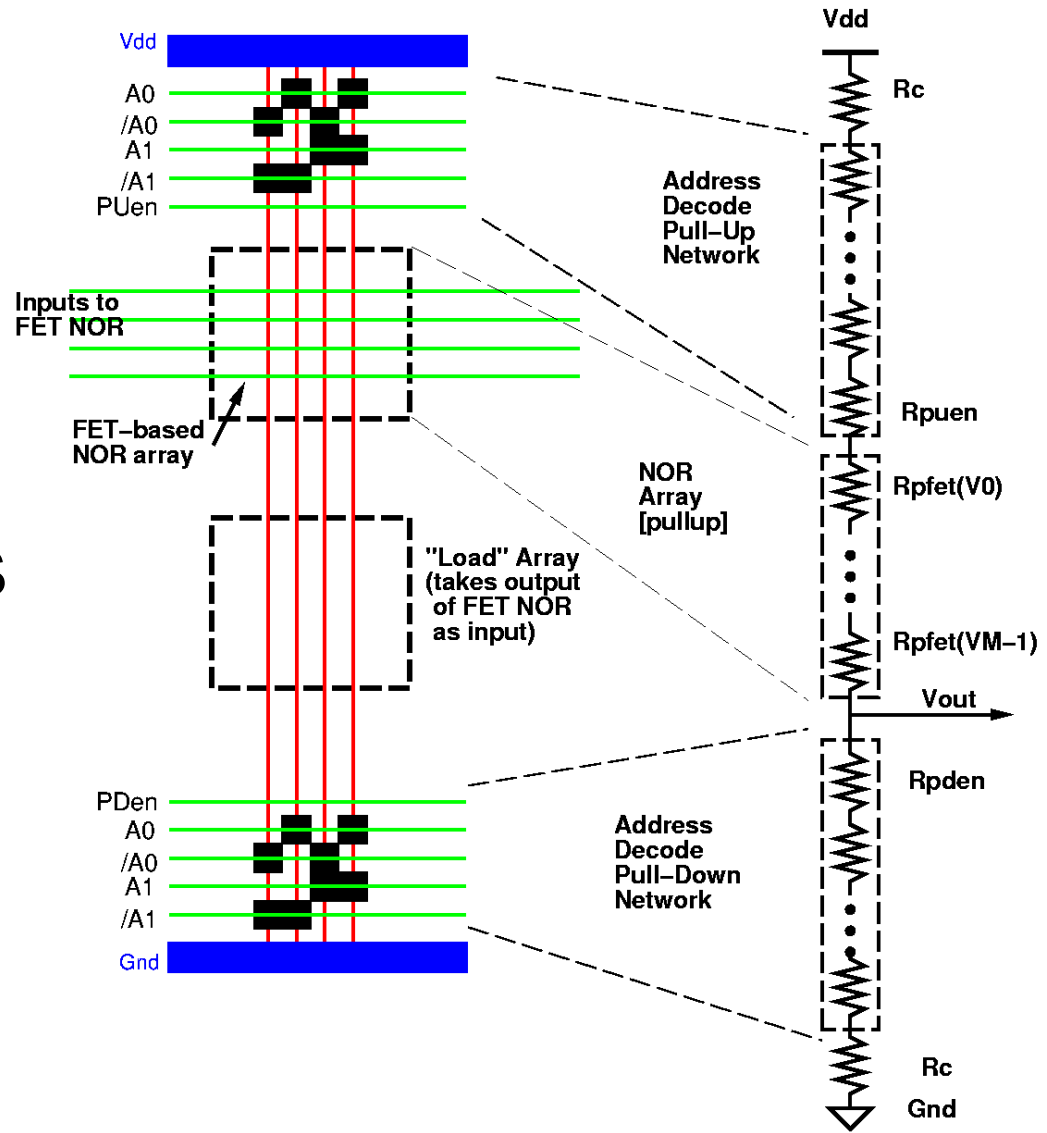


Recall PLA



Operating Array

- Decoders allow program array
 - OR, NOR
- Isolatable
- Dual role of loads during operation
- Output used directly by consumer



Codespace: How Large?

- How large does code space really need to be?
 - Addressing N wires
 - With code space $100N^2$
 - Has over 99% probability of **all** wires being unique
 - For logarithmic decoder:
 - Need a little over $2\times$ bits of sparse code

Array Size

- Larger crossbar
 - Amortize out microscale addressing overhead
- Smaller crossbars
 - Shorter wires
 - Less capacitance → faster, less energy
 - Less likely to fail
 - More efficient for logic

Array Size Summary

- Based on
 - Relative size of structures
 - Micro vs. nano
 - Overhead of current model
 - Current defect rate estimates
 - Modest arrays appropriate
 - 512 NT/NW per side
 - $A(512)=30$
 - $A_{\text{side}} = 30 \cdot 90\text{nm} + (512+11) \cdot 10\text{nm}$
 - 45-65% yield ?
 - 400-800 nm²/crosspoint
- 90nm DRAM
49,000 nm²
- 22nm DRAM
3400 nm²?