

# SH-Mobile3: Application Processor for 3G Cellular Phones on a Low-Power SoC Design Platform

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## Outline

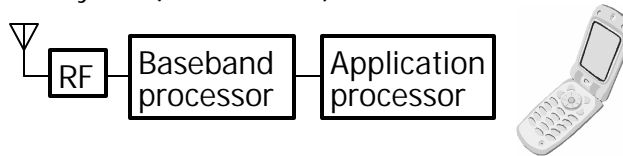
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- Background
- Chip overview
- Active power reduction
  - High MIPS/MHz CPU core
  - Java accelerator
- Standby power reduction
  - Low-power SoC design platform
  - Supply domains and two standby modes (Resume and ultra standby modes)
- Summary

# Background

## □ 3G cellular phone

- High data throughput (144k – 2M bps)
- Advanced applications (Java, videophone & 3D CG)
- Long battery life (> 300 hours)



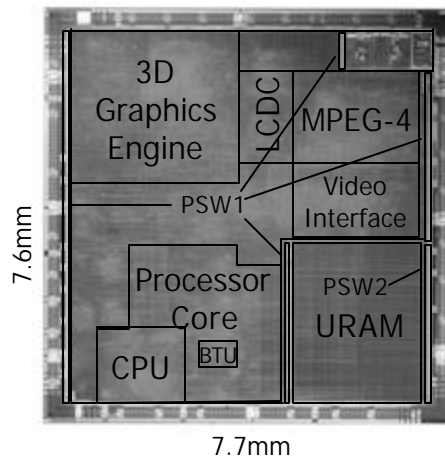
## □ Advanced process technology

- Higher operating speed, large amount of integration and lower leakage power are conflicting requirements.

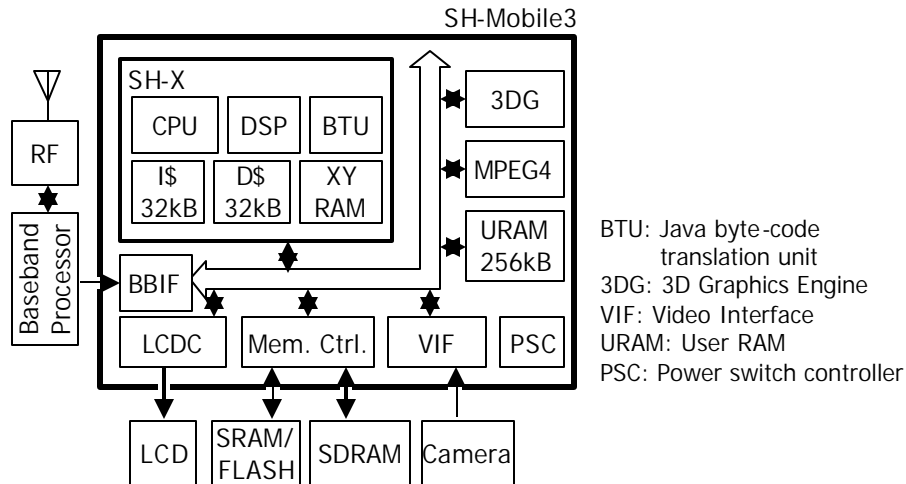
# Chip overview

The Java™, and all Java-based marks are trademarks or registered trademarks of Sun Microsystems, Inc. in the U.S. or other countries.

- 130-nm, Dual-Vth, Dual-tox CMOS (5Cu) technology
- Dedicated multiple computation engines:
  - SuperH CPU core (SH-X), inc. DSP & Java™ (BTU) engines
  - MPEG-4
  - 3D graphics
- 256-kB on-chip RAM (URAM)
- Low-power SoC design platform
  - $\mu$ I/O (level shifter technology)
  - On-chip power switches (PSWs)



## Chip diagram



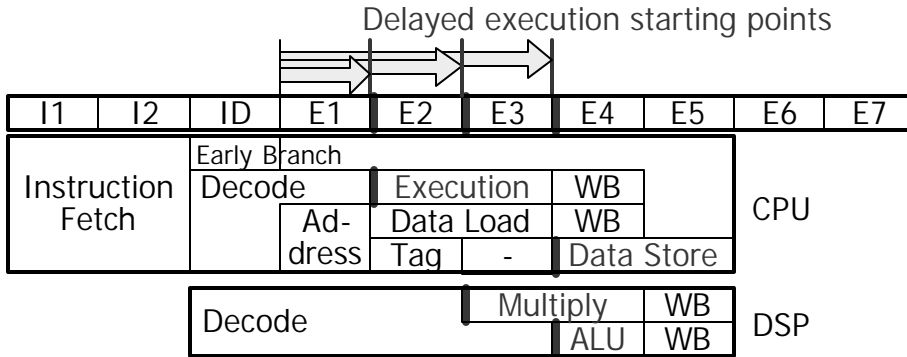
## Active power reduction

To achieve sufficient performance with minimum operation frequency and power consumption,

- High MIPS/MHz CPU core
  - Optimized dual-issue 7-stage pipeline
- Dedicated multiple computation engines
  - Java accelerator
  - MPEG-4
  - 3D graphics

# Pipeline structure

- Dual-issue 7-stage Pipeline
  - Higher MHz, but lower cycle performance
- Optimized pipeline using delayed execution enhances cycle performance.

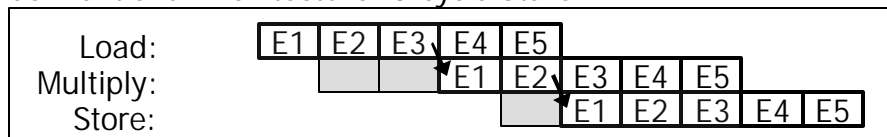


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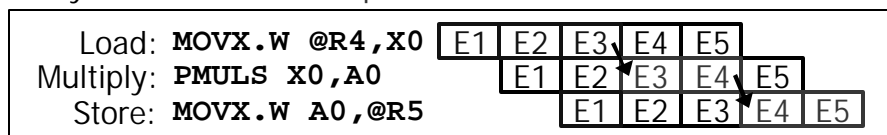
# Delayed execution (DE)

- DE accelerates multiple-cycle and dependent Inst. flows.
- e.g. typical DSP instruction flow:  
Load --- Arithmetic Executions --- Store

Conventional Architecture: 3-cycle Stalls

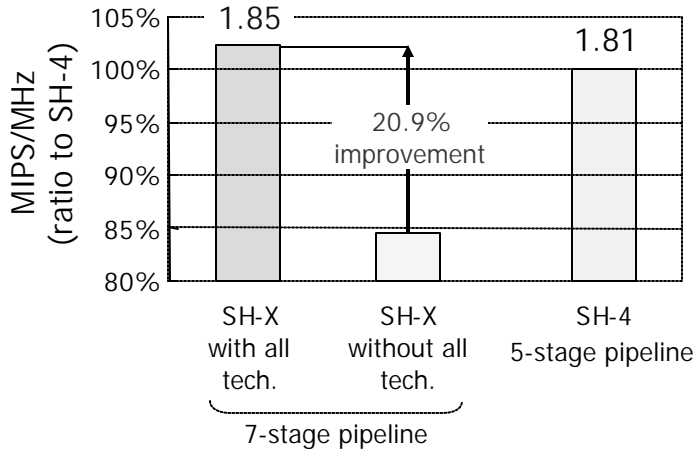


Delayed Execution: No Pipeline Stall



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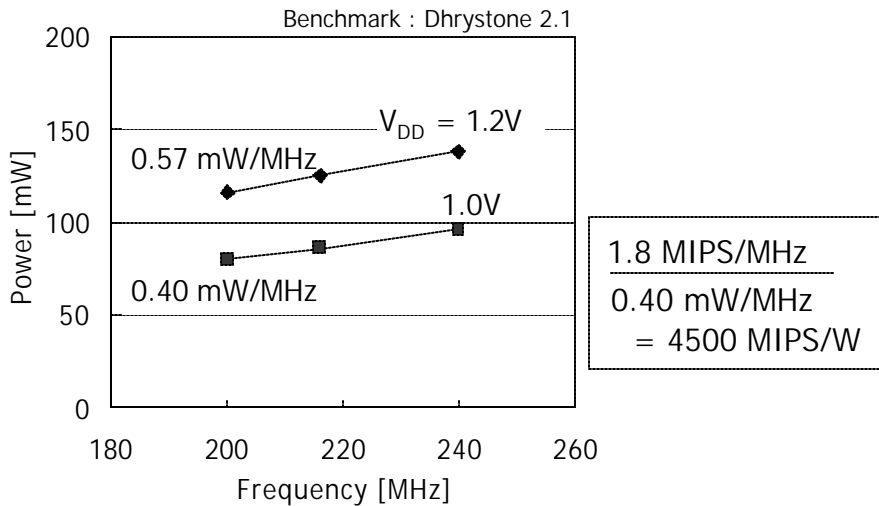
# Performance evaluation



Benchmark : Dhrystone 2.1 9



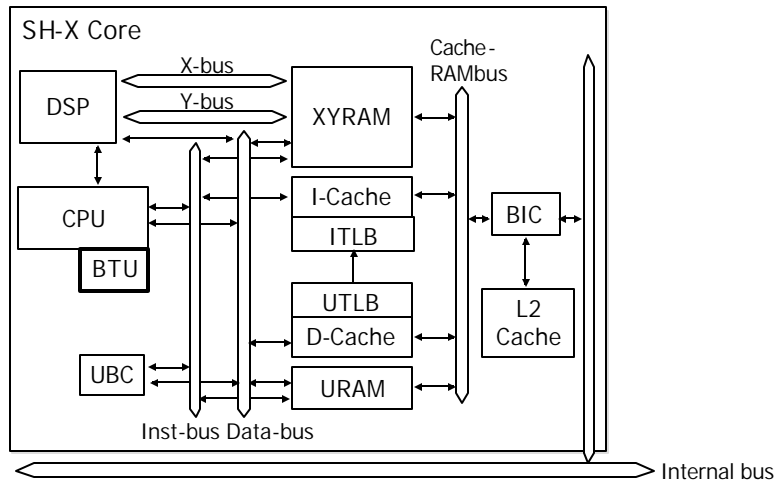
# Operating power of processor core



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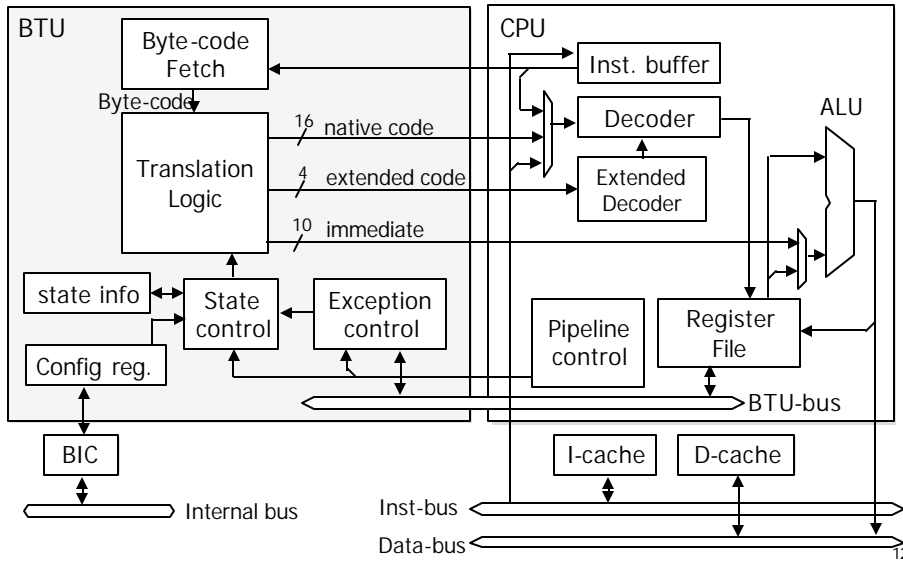


# Java accelerator (BTU)



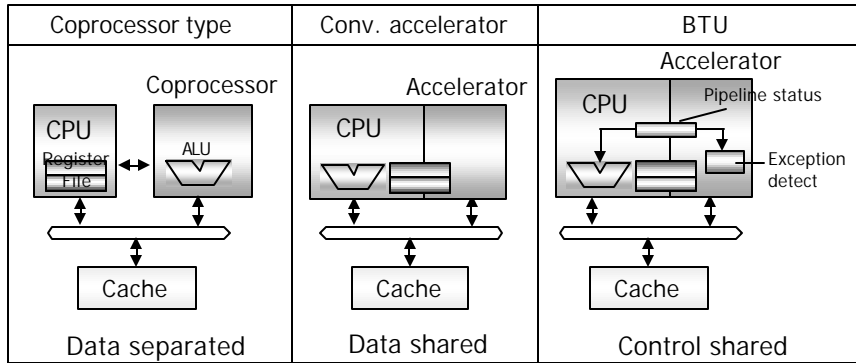
BTU: Java byte-code Trans. Units      URAM: User RAM  
 UBC: User Break Controller            BIC: Bus Interface Controller

# BTU block diagram



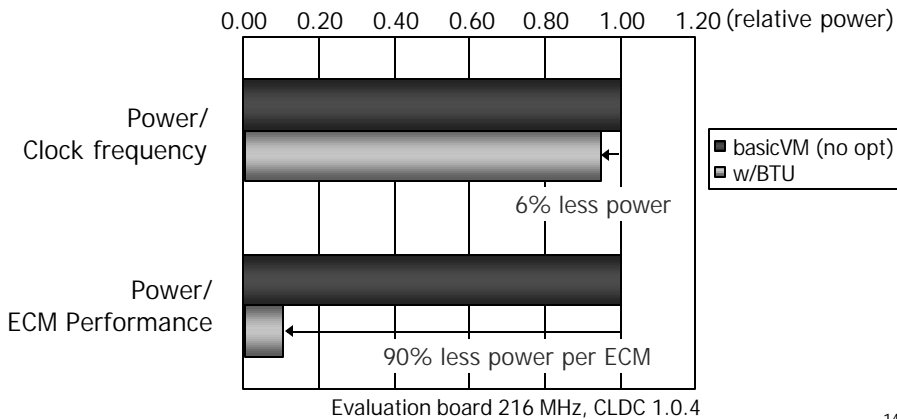
# Parallel execution in BTU

- BTU shares control information and data with CPU. It enables parallel execution of data and control processing. (e.g. Java exception detection)



# Java power evaluation

- Performance: w/BTU 6.55 ECM/MHz (basic VM 0.64 ECM/MHz)
- Power consumption is reduced by 6 %, and power/ECM is reduced by 90 %.



# Standby power reduction

To achieve lower standby power with minimum speed overhead,

## □ Low-Power SoC Design Platform

- On-chip power switches (PSWs)
- $\mu$ I/O
- Low leakage data-retention RAM technology

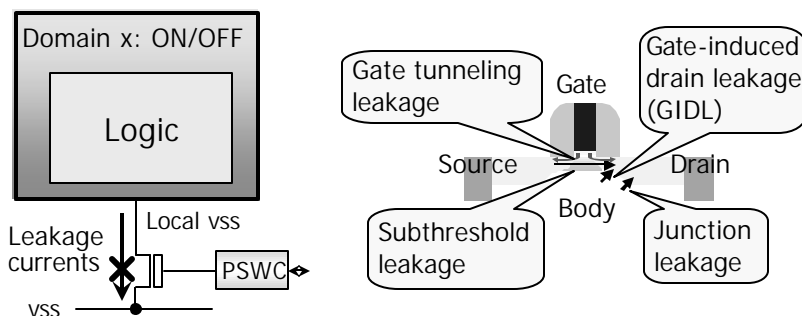
## □ Two Standby modes

- Resume standby mode
- Ultra standby mode



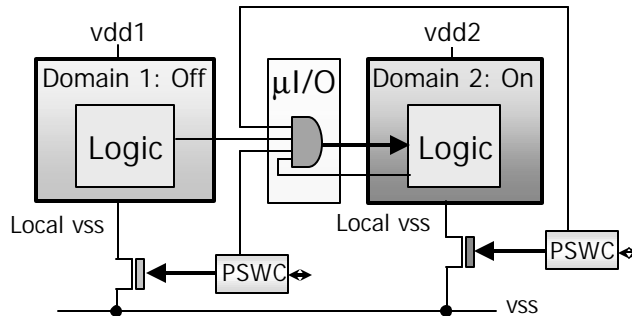
# Low-power SoC design platform (PSWs)

- Thick-tox High-Vth NMOS transistors are used for on-chip power switches (PSWs).
- It minimizes various leakage currents such as subthreshold, gate tunneling, GIDL, and junction leakage.



## Low-power SoC design platform ( $\mu$ I/O)

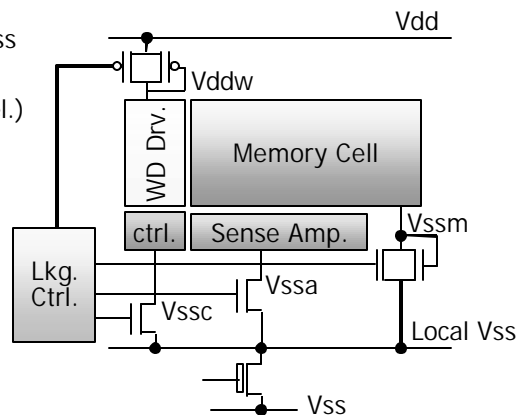
- $\mu$ I/O has level-shift function and provides optimal supply & voltage domains for dedicated multiple computation engines.
- It also prevents invalid signal transmission and supports:
  - Internal vss1 and/or vss2 shutdown by on-chip power switches
  - External vdd1 and/or vdd2 shutdown by off-chip regulators



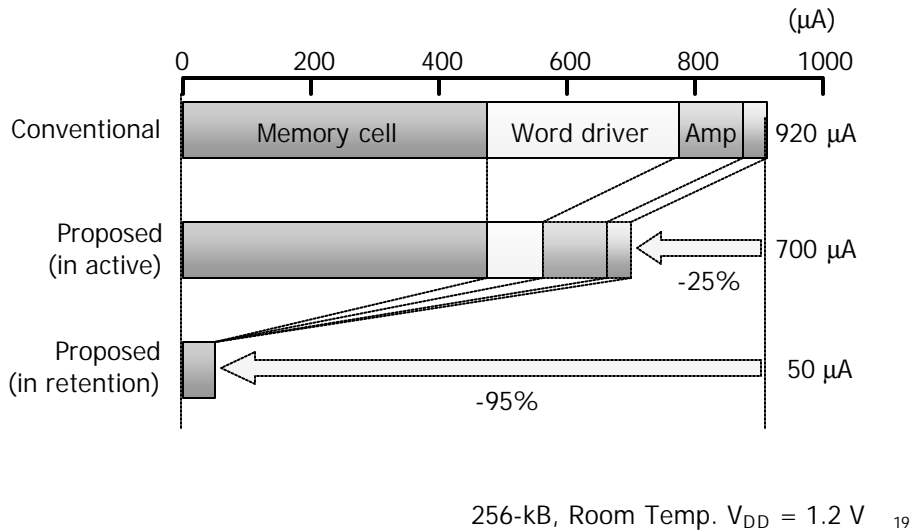
## Low-leakage data-retention memory

- Hierarchical on-chip power switches in SRAM provide subdivisinal power-line control.

- In active mode
  - Vssm, Vssa, Vssc = Vss
  - Vddw = Vdd (sel.)  
~0.4 V down (unsel.)
  - Local Vss = Vss
- In retention mode
  - Vssa, Vssc: Hi-Z
  - Vssm: ~0.4 V up
  - Vddw: ~0.4 V down
  - Local Vss = Vss
- In shut-down mode
  - Local Vss: Hi-Z



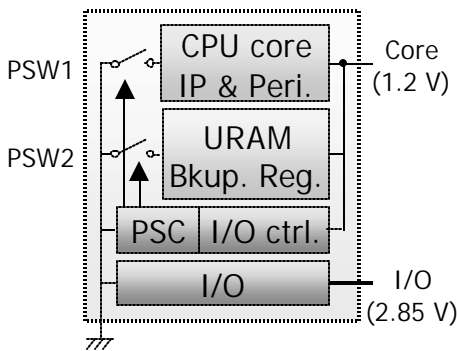
# Leakage current of the memory



# Two low-power modes

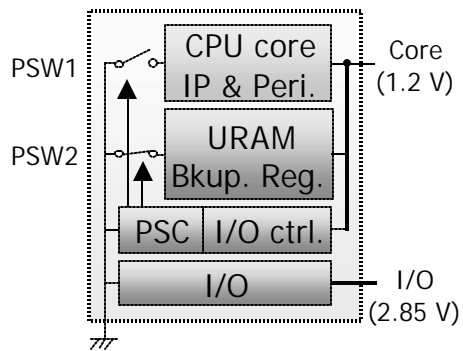
## Ultra standby

- Low leakage ( $\sim 10\ \mu\text{A}$ )



## Resume standby

- Low leakage ( $\sim 100\ \mu\text{A}$ )
- Quick recovery ( $< 3\text{ ms}$ )



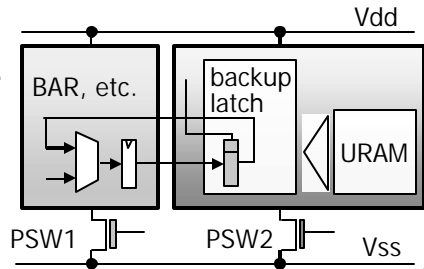
# R-standby recovery operation

## □ Hardware operation

- Power switch control
- Clock generation (PLL, D.PLL lock)
- Data backup using backup latch
  - BAR (Boot Address Register) holds restart address
  - Clock and interrupt setting needed just after wake-up

## □ Software operation

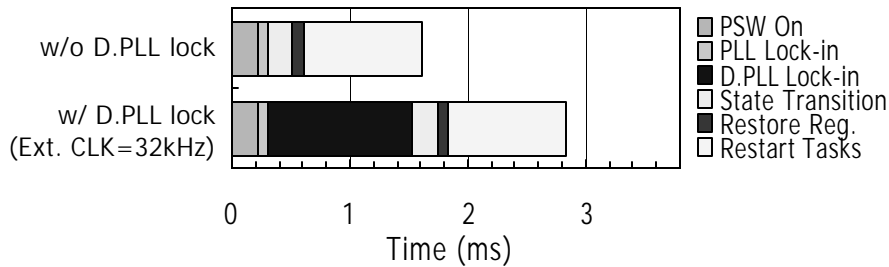
- URAM : data backup mem.
- Control registers
- OS task table
- etc.



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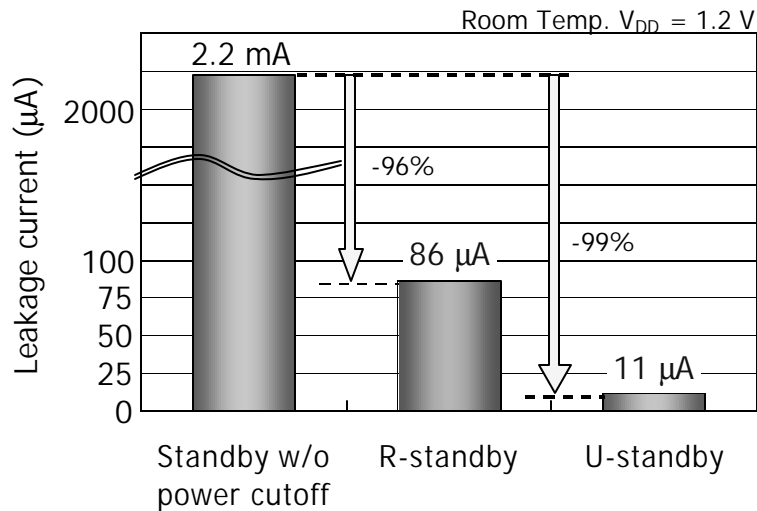
# Recovery time from R-standby

- Total recovery time from R-standby mode is only 1.6 ms or 2.8 ms (@Ext. clk=32 kHz).



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# Standby power consumption



# Summary

- 130-nm 5-layer-Cu dual-Vth, dual-tox CMOS technology
- Dedicated multiple computation engines:
  - SuperH CPU core (SH-X) including DSP & Java™ engines
  - MPEG-4
  - 3D graphics
- Power efficiency, SH-X: 4500 MIPS/W  
Java: 6.55 ECM/MHz
- Low-power SoC design platform
  - On-chip power switches
  - $\mu\text{I/O}$
  - Low-leakage data-retention RAM
- Two standby modes (R-standby and U-standby)
  - Leakage current: 86  $\mu\text{A}$  and 11  $\mu\text{A}$
  - Recovery time from R-standby: 1.6 ms or 2.8 ms (@Ext. clk=32 kHz)