



# Poulson: An 8 Core 32 nm Next Generation Intel® Itanium® Processor

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Intel®

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# Agenda

Design Space

Overview

Parallelism

Data Integrity

Power

Conclusion

# Design Space: Mission Critical

## Performance

- Both single-thread speed and total throughput are important
- Goal: > 2x generational performance improvement

## Scalability

- Glueless up to 8 sockets
- Support larger topologies via node controllers from system vendors

## Reliability

- Redundancy and self-correction
- Error detection and recovery via hardware and firmware

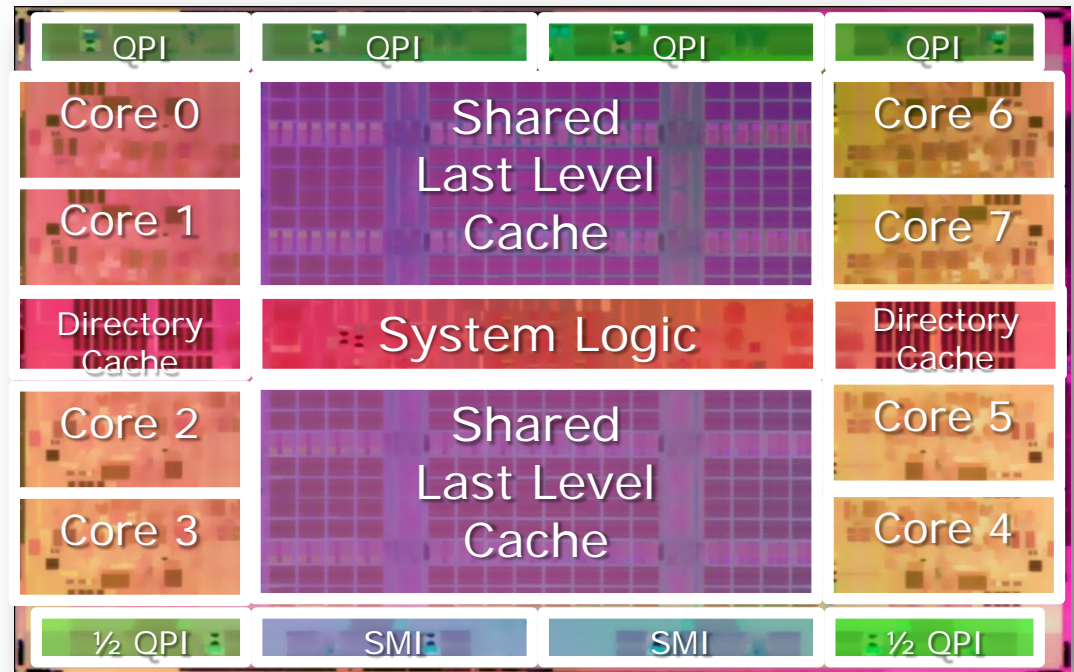
## Compatibility

- Socket compatible with Itanium® 9300 Processor Series (Tukwila)
- Common platform ingredients with Xeon® E7 Processor Series

# Poulson Overview

	Tukwila	Poulson
Process	65nm	32nm
Devices	2.05 Billion	3.1 Billion
Area	700 mm <sup>2</sup>	544 mm <sup>2</sup>
Power (max TDP)	185W	170W
Itanium <sup>®</sup> Cores	4	8
Last Level Cache Size	24MB	32MB
Intel <sup>®</sup> QuickPath Interconnect Links	4 full + 2 half	4 full + 2 half
Intel <sup>®</sup> QPI Link Speed	4.8GT/s	6.4GT/s
Intel <sup>®</sup> Scalable Memory Interface Links	4	4
Intel <sup>®</sup> SMI Link Speed	4.8GT/s	6.4GT/s

# Poulson Overview



8 Itanium® Cores

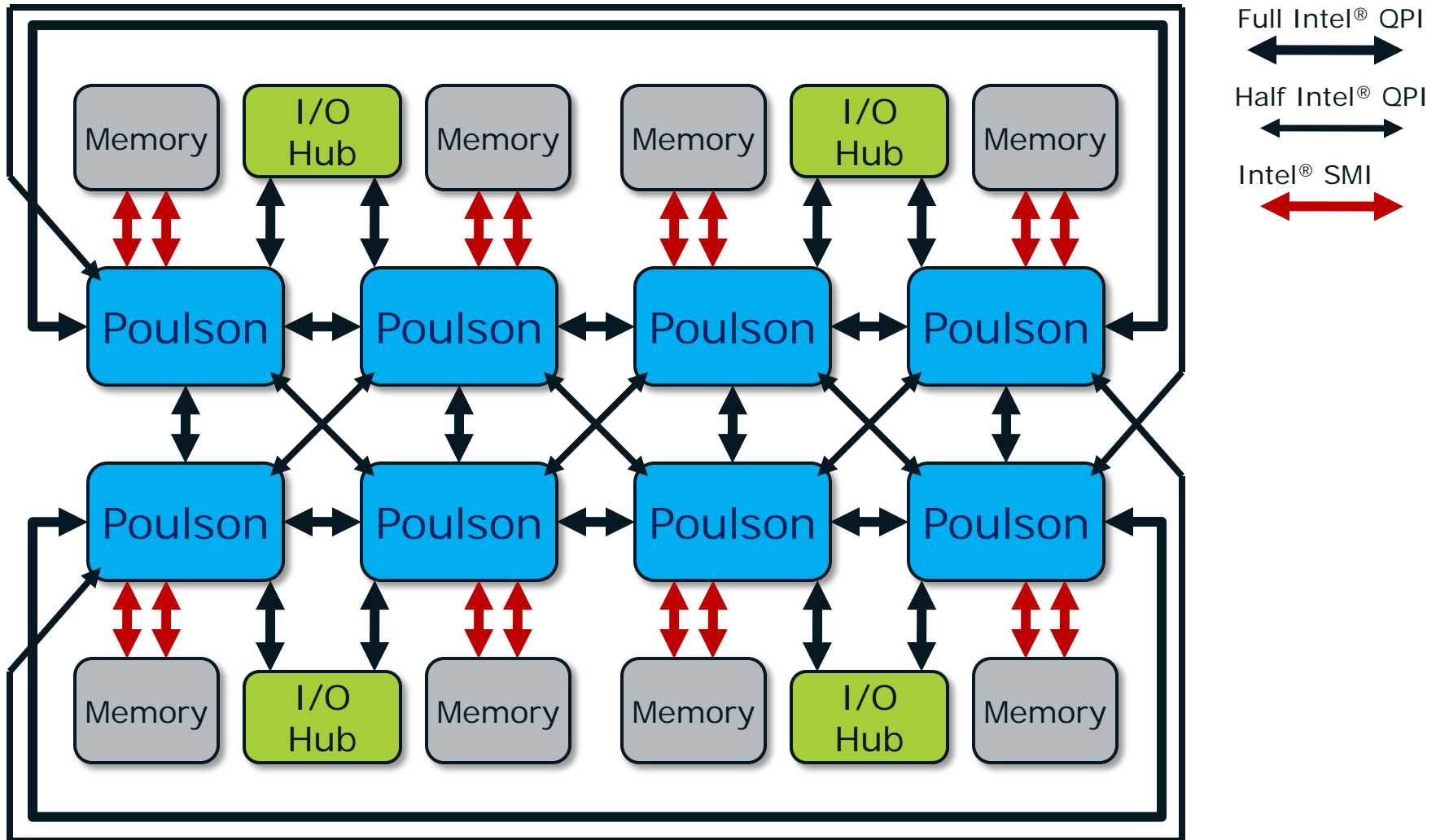
32MB Last Level Cache

4 full-width and 2 half-width Intel® QPI links

2 Directory caches

2 Integrated memory controllers with 2 Intel® SMI links each

# Example 8-Socket Topology



# Poulson Core

	Tukwila	Poulson
Devices	108 million	89 million
Area	69 mm <sup>2</sup>	20 mm <sup>2</sup>
Process scaled power @ TDP	1.0	0.4
Process scaled frequency	1.0	>1.2
Threads	2	2+2
Instruction Q size	48	96x2
Max instruction issue/cycle	6	12
Pipeline stages	2 + 6	4 + 7
Pipeline hazard resolution	Interlock+Stall	Replay
Integer RF size	144	185
Integer RF ports	12R 8W	12R 12W
RF protection	Parity	SECDED

**All-new Itanium® core**

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# Itanium® New Instructions

## Integer operations

- mpy4
- mpyshl4
- clz

## Thread Control

- hint@priority

## Expanded Data Access Hints

- mov dahr

## Expanded Software Prefetch

- lfetch.count

# Exploiting Parallelism on All Levels

Instruction Level Parallelism

Memory Parallelism

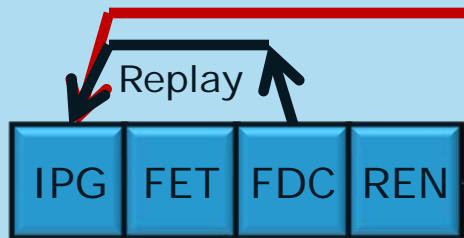
Thread Parallelism

Multi-core Parallelism

**Multi-level parallelism exposed to software control**

# Instruction Parallelism

## Front-end Pipeline

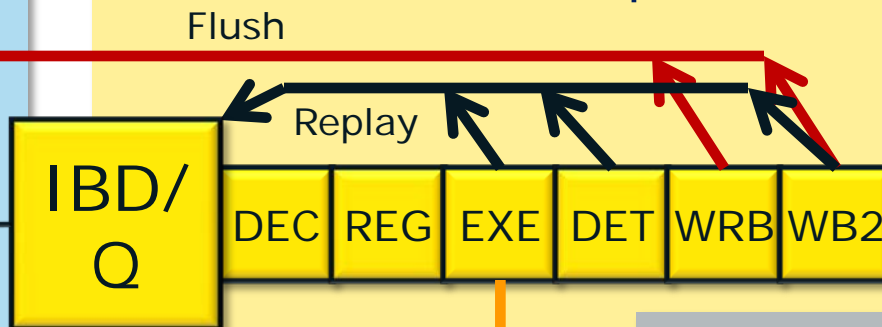


IPG: Address Gen  
 FET: Array Access  
 FDC: Early Decode  
 REN: Register Rename

Fetch width: 32B/cycle  
 Multi-level branch Prediction  
 Renaming: 128 logical to  
 185 physical registers

Independent thread domain

## Main Pipeline



IBD: Instr Buffer/Dispersal  
 DEC: Instr Decode  
 REG: Register Read  
 EXE: Execute  
 DET: Exception Detect  
 WRB: Write-back  
 WB2: Commit

Q holds 96 instructions  
 In-order issue

Independent thread domain

## MLD Pipeline



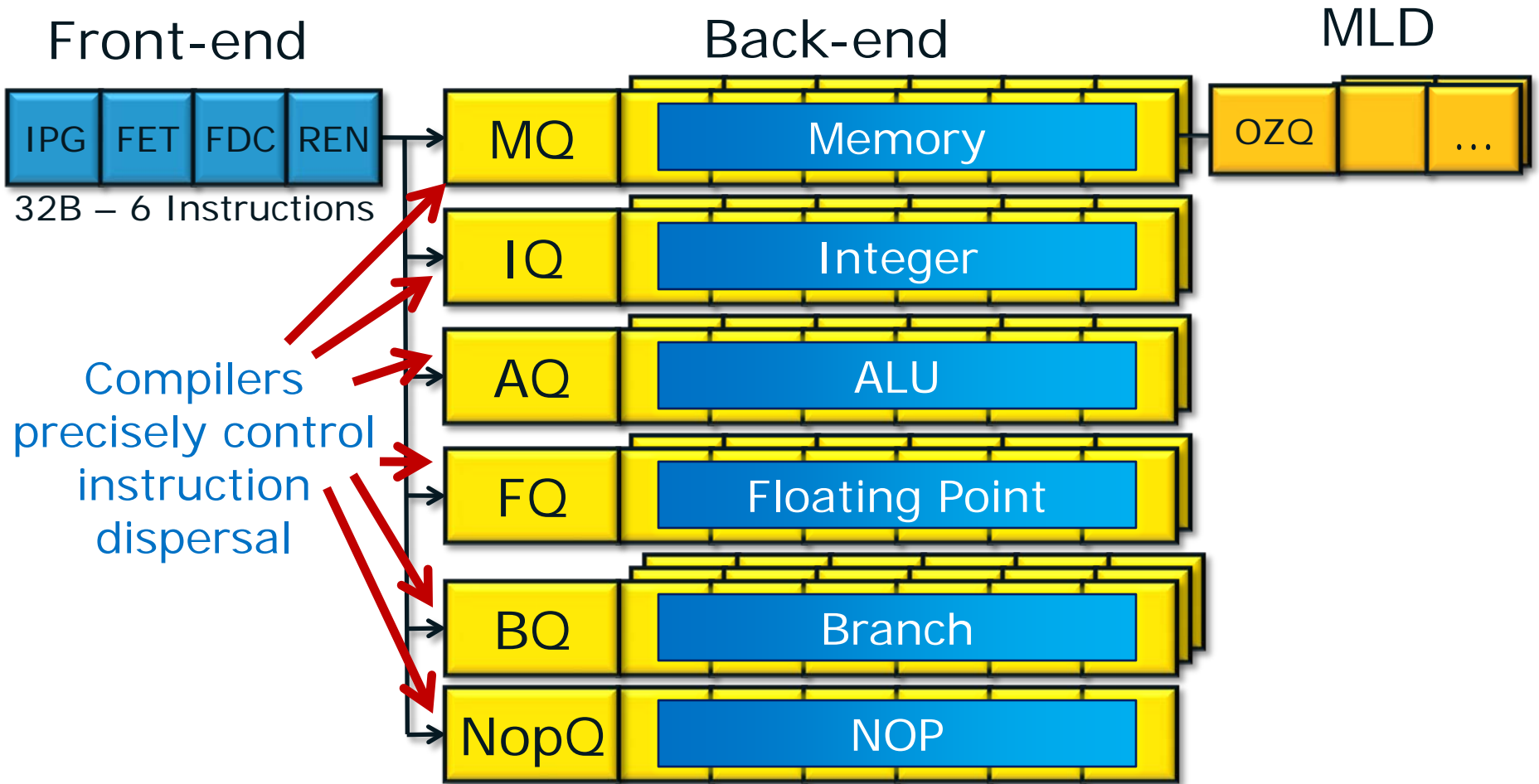
MLD: Mid-level data cache  
 OZO: Architectural memory  
 ordering queue

OZO holds 16 memory ops  
 OOO issue

Independent thread domain

## Concurrency via 3 decoupled pipelines

# Instruction Parallelism



**12-wide issue under software control**

# Memory Parallelism – Avoiding Hazards

## Expanded Software Hints

- Provides control over allocation, speculation and prefetch policies
- Multi-line software prefetch

## Reduced Speculation Costs

- Spontaneous Deferrals on speculative loads
- Deferred load can transform into a prefetch to cache and/or TLB

## New Hardware Prefetcher

- Into FLD and/or MLD
- Adaptive based on FLD/MLD miss patterns

## Reduced Data Hazards

- Expanded store to consumer bypassing in FLD and MLD
- Single-cycle MLD to FLD line transfers

**Pipeline bottlenecks removed**

# Memory Parallelism – Increasing Throughput

More pending memory operations in each core

- Increased from 48 to 64 operations in MLD
- Increased from 44 to 80 operations in Ring interface

Ring Cache

- 8 Independent LLC pipelines and controllers per socket
- 2 caching agents per socket to generate Intel® QPI transactions

Increased Intel® QPI link bandwidth for multi-socket throughput

Memory Subsystem Improvements

- Home agent in-flight transaction tracker increased by 50%
- MC scheduler algorithm changes focused on performance and power efficiency
- Intel® SMI link speed increased

**Improved queuing and B/W**

# Thread Parallelism

Intel® Hyper-Threading Technology with Dual Domain Multithreading support

- Front-end and main pipelines are independently threaded
- Pipeline-specific thread switch mechanisms

More per thread resources

- Instruction queues
- Data TLBs
- Hardware page walker handles concurrent walks to both threads

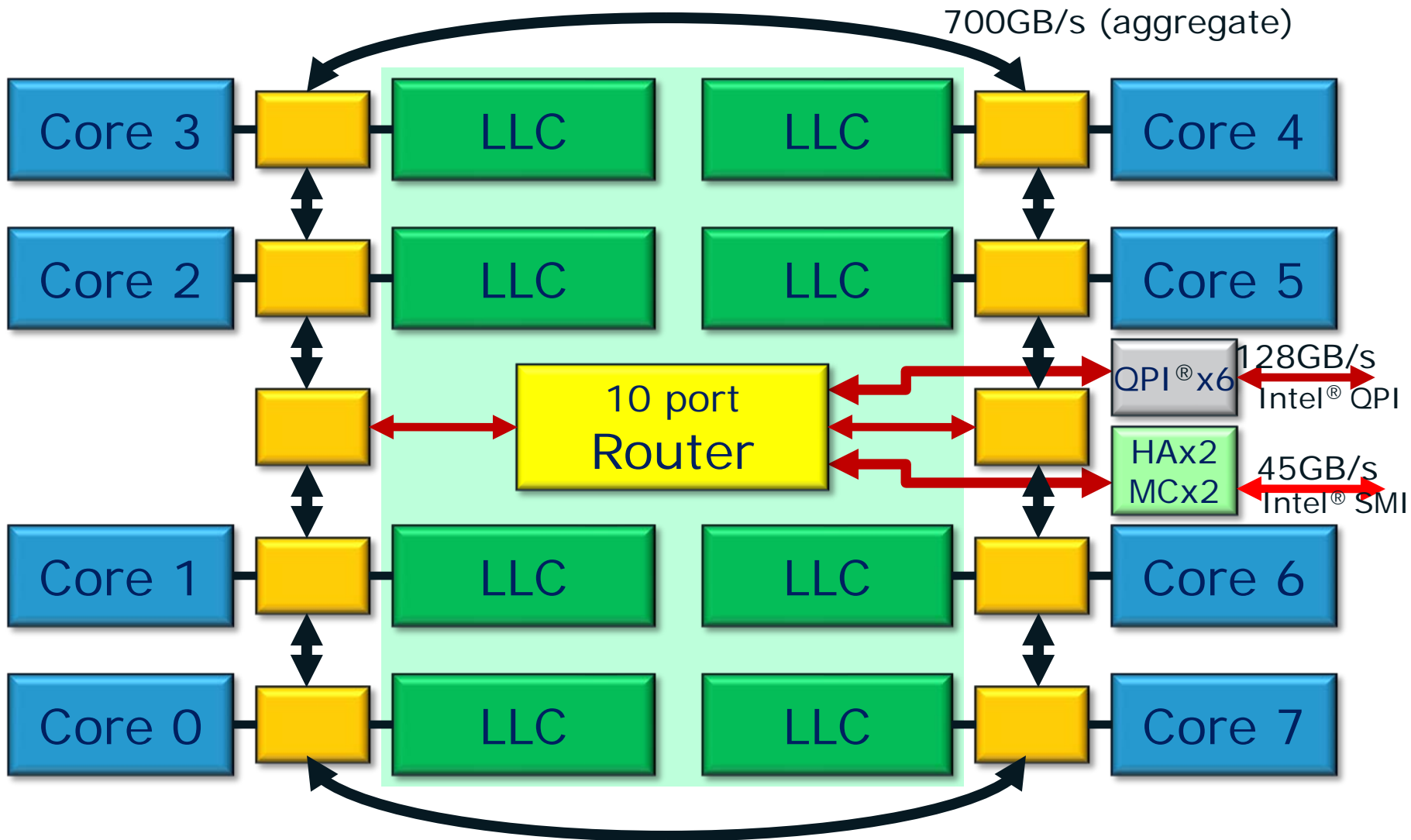
Instructions provide software hints to thread switch hardware

Attention to Thread Fairness

- Hardware to identify unfair behavior
  - Measures instruction retirement and data cache resource usage
- Firmware configurable responses to unfairness
  - By biasing towards victim thread

**Increased throughput via improved threading**

# Multi-core and Multi-socket Parallelism



# Reliability, Fault Tolerance and Recoverability

## Intel® Instruction Replay Technology

- Main pipeline redesigned for error handling
- Enabled hardware and firmware recovery of correctable errors

## Increased Error Detection and Correction

- Arrays
  - MLI, MLD, LLC tag and Directory cache – SECDED
  - LLC data – DECTED
  - Register files (GR and FR) – SECDED
- Logic path error detection in FP ALU via residues
- Key paths are protected “end to end” with invalidation and replay

## Reworked Error Detection, Response and Reporting Framework

- Large increase in error detection and response capabilities
- Increased hardware responses and recovery
- Intel® Cache Safe Technology: lockout of failing cache locations

# Power Aware Design

## Replay-based Pipeline

- Enabled fully gated clocks
- Eliminated slow and power-wasting global pipeline stalls

## Aggressive Clock Gating

- Substantial reductions in both idle, typical and max power

## Removed Dynamic Logic from FPU

## Low-Leakage FETs

## Digital Power Prediction

- Measures, weights and averages key core state signals
- Beyond architectural state – uses data patterns
- Estimation error decreased from 35% to 2%

**60% TDP, 70% idle  $C_{dyn}$  reduction  
over process scaled Tukwila**

# Poulson Status

Well into post-Si validation

Booted and being tested on multiple operating systems

Running in many topologies

On track for 2012 shipments

# Conclusion

## All new core design

- 12-wide issue
- Intel® Hyper-Threading Technology with Dual Domain Multithreading
- Itanium® New Instructions and policies for fine-grain software control of hardware parallelism
- Intel® Instruction Replay Technology for frequency, power and fault tolerance
- Core power efficiency: > 3x better than Tukwila<sup>1</sup>

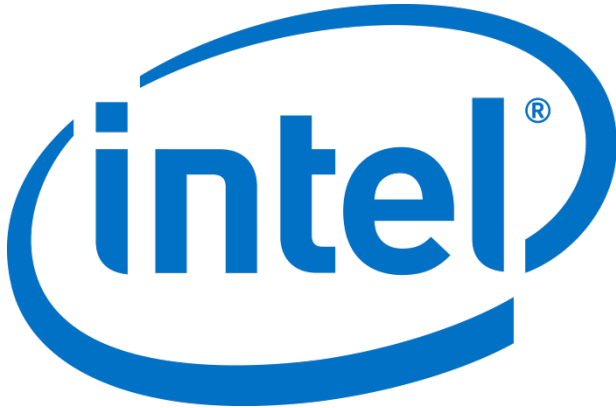
## Ring-based design

- Large last level caches
- High bandwidth system interface

## Outstanding data reliability

- Enhanced error detection
- Improved error recovery
- Better RAS integration

1 – Internal lab measurement



# Glossary

<b>DECTED</b>	Double Error Correction, Triple Error Detection
<b>DTB</b>	Second Level Data TLB
<b>FIT</b>	Failure in Thousands
<b>FLB</b>	First Level Branch Cache
<b>FLD</b>	First Level Data Cache
<b>FLI</b>	First Level Instruction Cache
<b>HA</b>	Home Agent: Intel QPI agent responsible for managing memory
<b>ILP</b>	Instruction Level Parallelism
<b>IPF</b>	Itanium® Processor Family
<b>LLC</b>	Last Level Cache
<b>MC</b>	Memory Controller

<b>MLD</b>	Mid Level Data Cache
<b>MLI</b>	Mid Level Instruction Cache
<b>OZQ</b>	Ordering cZar Queue: architectural memory ordering
<b>QPI</b>	Intel® QuickPath Interface
<b>RAS</b>	Reliability, Availability and Serviceability
<b>RF</b>	Register File
<b>SECTED</b>	Single Error Correction, Double Error Detection
<b>SMI</b>	Intel® Scalable Memory Interconnect
<b>TDP</b>	Thermal Design Power
<b>TLB</b>	Translation Look-aside Buffer