

**THE LR33020 "GRAPHX" PROCESSOR:  
A MIPS-RISC BASED GRAPHICS PROCESSOR  
FOR X-TERMINALS**

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**AGENDA**

- **Technical Design Goals**
- **Target Applications**
- **Feature Overview**
- **Example X-Terminal Systems using LR33020**
- **Performance**
- **Summary**

## TECHNICAL DESIGN GOALS

Design a Solution for High-End, Low-Cost, Graphics Control Applications that:

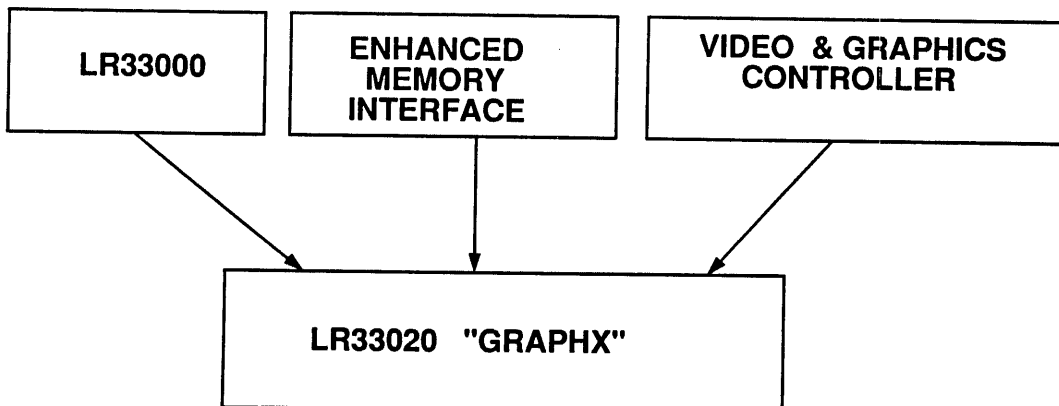
- Retains the Strengths of the MIPS Architecture:
  - High Performance over Several Applications
  - Usage of the MIPS Compilers and Development Tools
- Builds Upon the Advantages of the LR33000 Implementation:
  - High Integration and Minimal System Cost
  - Simple System Design
- And Adds Value (for Graphics Applications & X-Terminals) by:
  - Integrating Graphics and Video Control Functions
  - Providing Increased Bandwidth to Memory
  - Tightly Coupling the CPU and Graphics H/W to Minimize Overhead

*low-end  
2D graphics  
applications*

*R3000 MIPS 1  
compatible*

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## CONCEPTUALLY "GRAPHX" IS:



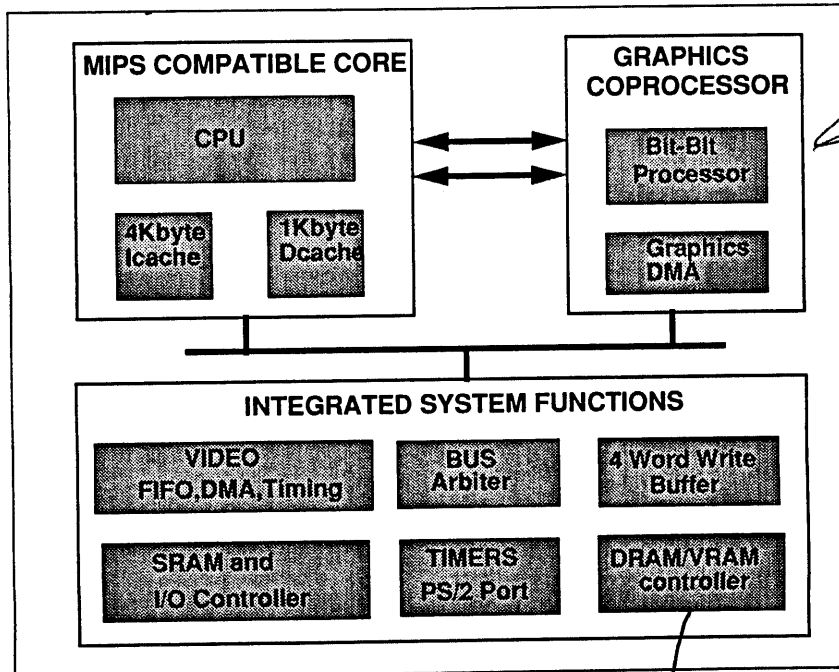
## TARGET APPLICATIONS

- X-Window Terminals *← primary application*
- Laser Printers
- PC Graphics Add-In Cards
- Work Station Frame Buffer Controllers
- High Performance Plotters and Printers

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224 PIN PGA  
208 PIN MQAD

## LR33020: SIMPLIFIED BLOCK DIAGRAM



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64-50 PPGA

3.2.3

## FEATURE OVERVIEW

- **Modified LR33000 Functionality:**
  - R3000 Compatible CPU Core
  - 4K Byte Instruction Cache and 1K Byte Data Cache
  - Two Counter/Timers
  - 4 Deep Write Buffer
- **Graphics and Video Support:**
  - Dedicated Bit Blit Coprocessor (BBCP)
  - Flexible Video Timing Generation
  - Video Data FIFO for DRAM Based Frame Buffer - can double as h/w cursor storage for VRAM based Frame Buffer systems
  - 4 DMA Channels for Pixel Moves and Display Refresh

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## FEATURE OVERVIEW (contd.)

- **Enhanced Memory Interface:**
  - Direct Support of Interleaved DRAM (64 bit datapath to external memory)
  - VRAM Support
  - Direct Interface to 8 bit PROMs
  - Minimizes External Programmable Devices
  - 4 Independent Regions with Programmable Wait State Generation

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## BIT BLIT COPROCESSOR (BBCP)

- Implemented as MIPS Coprocessor2:

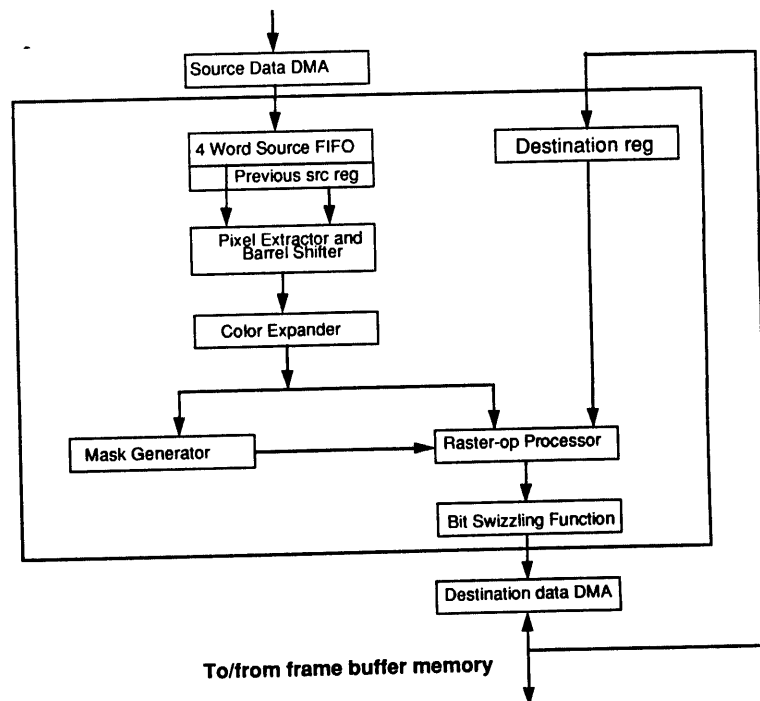
Uses Coprocessor Instructions: MTC2, MFC2, SWC2, LWC2  
for Transfers Between BBCP Registers, CPU Registers, and Memory

Uses newly defined Coprocessor 2 instructions for sequencing pixel data  
through the bit-bit datapath

- Performs Source to Destination Data Moves with Bit Alignment
- 16 Function Logical Unit
- Supports Color Expansion for Efficient Font Bit Maps
- Hardware Support for Bitmap Transparency
- Supports Various Pixel Sizes: 1, 2, 4, 8, 16, 32 Bits
- Utilizes Two DMA Channels to Control Bit Block Transfers
- BBCP Data is not Cached
- BBCP Data Utilizes Burst Mode Write Bypassing Write Buffer

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## BBCP DATAPATH



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## BBCP INSTRUCTIONS

- Utilizes Cop 2 "Draw and Step" Instructions: SSTEP, WSTEP, BSTEP, SBSTEP
- Control Data Transfers through BBCP
- Each Step Instruction Moves 1 or 4 Words
- DMA Channel Does Address Generation, DRAM Controller Handles Execution
- Pipelined Operation Enables Optimizing Performance:

Three Step Instructions Can Be Present in COP2 Pipeline  
without Stalling CPU

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## BBCP INSTRUCTIONS (contd.)

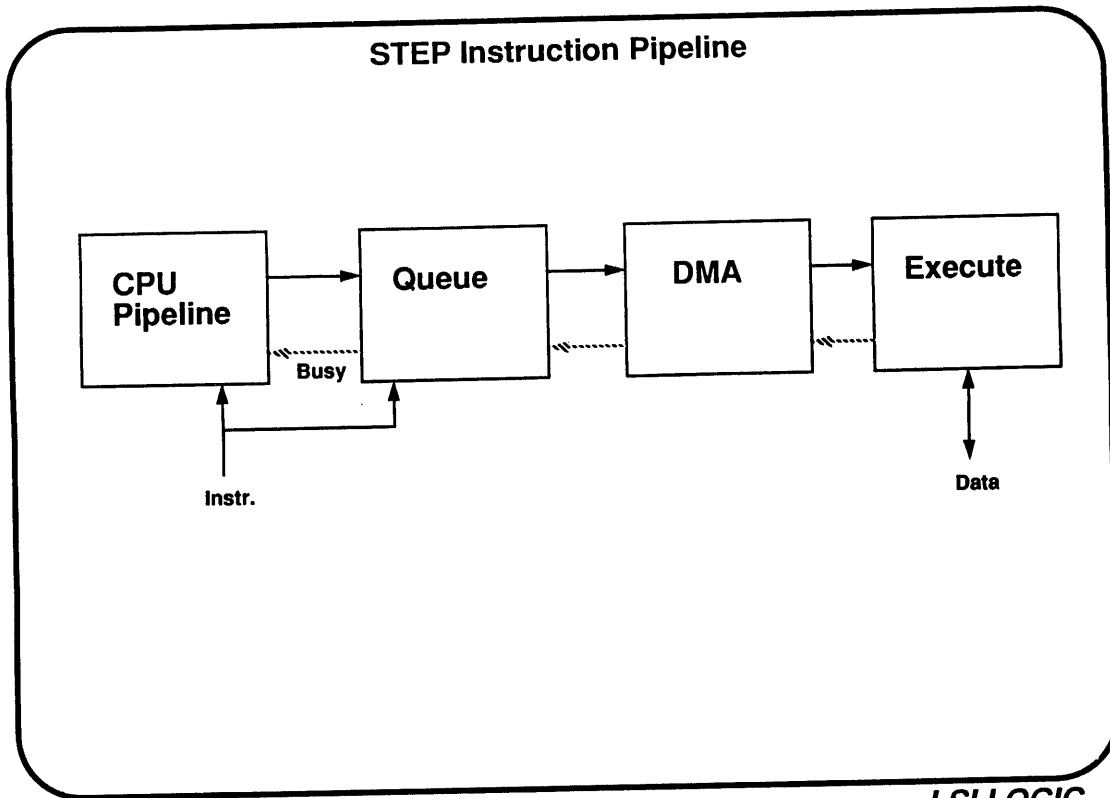
**SSTEP :** Steps to the next word in the Source queue. If queue empty initiate another DMA fetch of the source pixel data

**WSTEP:** Write the processed pixel word back to the current destination location

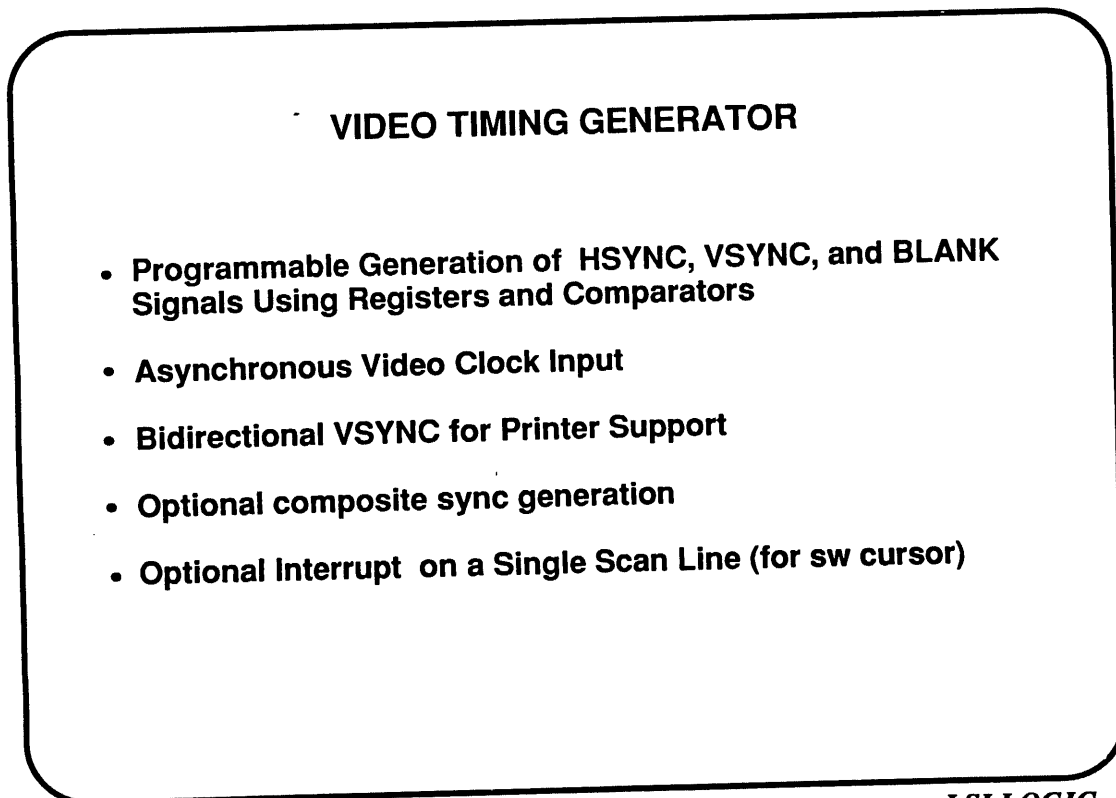
**BSTEP:** Step to the beginning of next destination line and write the processed pixel word

**SBSTEP:** Clears the source queue, step to the beginning of next source line and initiate another DMA fetch of source pixel data

The WSTEP and BSTEP instrs have optional flags to take care of boundary conditions and special VRAM functions (eg. block write)



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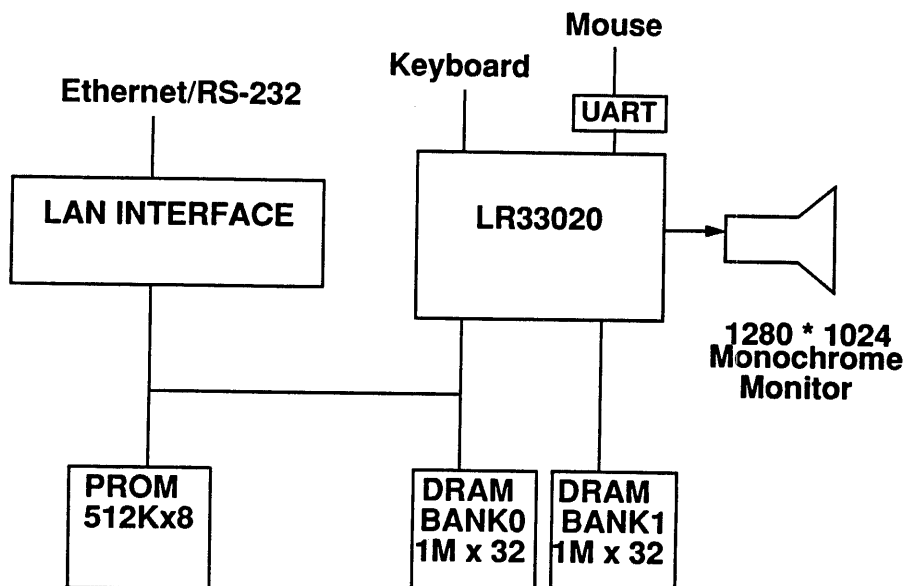
## VIDEO FIFO

- 32 by 32 Bit FIFO and Video Shifter
- Targeted at Low Cost DRAM only Based Systems for:
  - High Resolution Monochrome Displays
  - Medium Resolution Color Displays
  - High Resolution Monochrome Laser Printers
  - High Resolution Color Laser Printers
- DMA Controller Transfers Blocks of Refresh Data to FIFO from DRAM to Minimize Bus and CPU Overhead
- Serial Data Output: 1, 2, 4, 8 Bits/Clock Period
- Implements 64\*64\*2 Hardware Cursor in VRAM Based Systems

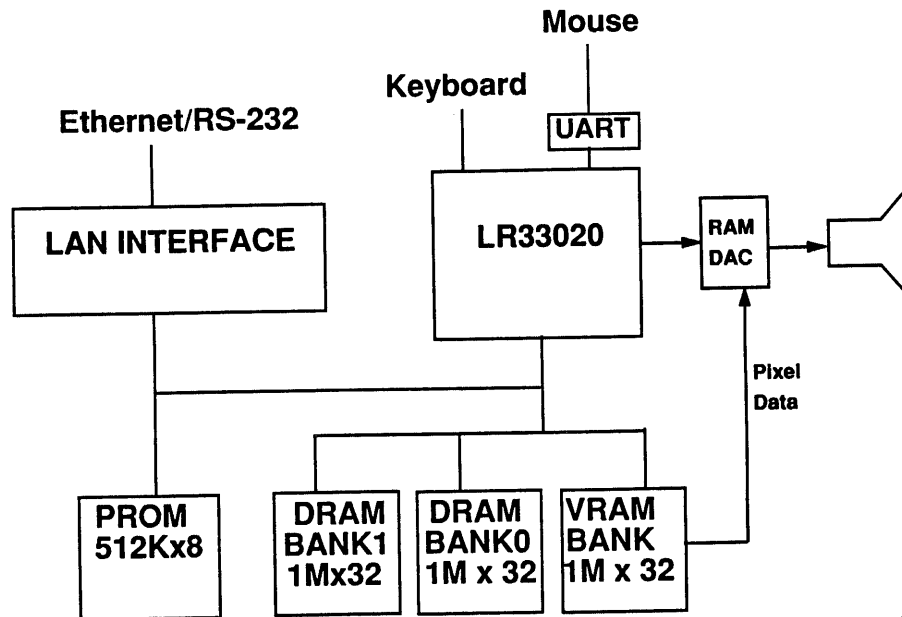
*NO VRAMS FOR  
CMT systems*

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## LR33020 Based MONOCHROME X-TERMINAL SYSTEM



## LR33020 Based COLOR X-TERMINAL SYSTEM



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### Performance

<u>Object</u> (Kobj/sec) (8 bit/pixel system)	<u>LR33020</u> 33mhz	<u>Magnum</u> 33mhz	<u>DECCfb</u> 33mhz	<u>DECSfb</u> 33mhz	<u>HP</u> 66mhz
10x10 Solid FILL	147	39	88	145-213	278
10x10 Stippled FILL	101 <sup>a</sup> /140 <sup>b</sup>	22.6	34	96-155	136
10x10 Opaque st. FILL	105	34.9	31	96-129	136
10x10 COPY	55.4	10.3			
100x100 Solid FILL	8.5	1.78			
100x100 Stippled FILL	1.751	.767			
100x100 COPY	2.1	1.0			

a: without VRAM block write

b: using VRAM block write

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## PHYSICAL CHARACTERISTICS

**Frequency:** 25, 33, and 40MHz Versions  
**Package Styles:** 208 Pin MQUAD and 224 Pin CPGA  
**Power:** 2.5W at 25MHz to 4.0W at 40MHz  
**Technology:** LCB007 (0.7u l-effective), 2 layer metal, std. cell  
**Transistors:** ~500,000

*10 SAMPLE STATE  
OF INTEGRATION*

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## SUMMARY OF FEATURES

- Targeted For High-End, Low-Cost, Graphics Controller Applications
- High Integration: CPU+I/D Cache+Timers+Memory Controller+Graphics+Video
- Software Compatible with R3000
- Graphics Extensions Provided By Coprocessor Instruction Set
- Directly Interfaces with VRAMs, Interleaved DRAMs, SRAMs, 8 Bit PROMs
- 25MHz, 33MHz, and 40MHz Versions
- Single 1X Clock Input
- Reduced Power Consumption: 2.5W at 25MHz
- Implemented in 1 Micron Drawn, Cell Based Technology: LCB007