

August 14, 1994 — Memorial Auditorium

Sunday Tutorial Schedule

- 7:30 – 8:30 Registration & Coffee at Memorial Auditorium
- 8:30 – 12:00 Algorithms and Hardware for Video Compression
- 12:00 – 1:00 Lunch
- 1:00 – 4:30 Instruction-Set Extensions for Multiprocessor Interconnects
- 4:30 – 6:30 Wine & Cheese Reception in the Dohrmann Grove
just north of the Hoover Tower on Serra Street.

Additional On-Site Registration will be available for an hour before the sessions begin on Monday and Tuesday.

Algorithms and Hardware for Video Compression Teresa H. Meng, Stanford University

This tutorial will give an overview of the industry standards for video compression, including compression algorithms, performance comparisons and hardware implementations. Fast algorithms to achieve real-time encoding and decoding will be one focus of this tutorial. Besides industry standards, recent developments in compression techniques, such as subband and wavelet filtering and vector quantization will be covered. Finally research activities in the area of low-power implementations for portable video applications will be surveyed.

Instruction-Set Extensions for Multiprocessor Interconnects David V. James, Apple Computer

Most instruction sets have been optimized for uniprocessor environments. To effectively utilize multiprocessors on scalable interconnects, processors need to support additional capabilities, including 64-bit addressing, a well-defined set of memory-access capabilities (loads, stores, and locks), non-blocking interrupts and synchronized time-of-day clocks. As background, the constraints of a typical high-speed interconnect, ANSI/IEEE Std 1596-1992 Scalable Coherent Interface (SCI), are considered. We show that specialized signals (such as bus-lock and interrupt) as well as eavesdrop or broadcast-based protocols can be avoided, explicit lock instructions (such as fetch&add) scale better than LoadReserved- and StoreConditional-based instruction sequences, and mixed endian data types (big and little) require minimal hardware (but significant compiler) support. We show how these considerations impact the design of processor instruction-set extensions.

Organizing Committee for HOT Chips VI

General Chair

John Mashey, Silicon Graphics

Program Committee Co-Chairs

Donald Alpert, Intel

Alan Jay Smith, UC Berkeley

Vice Chair

Nam Ling, Santa Clara University

Local Arrangements

Alan Johnson

Cary Kornfeld, Interval Research

Registration

Robert Stewart, Stewart Research Enterprises

Publications

David Gustavson, SCI Technical Consortium

Finance

Dennis Reinhardt, Intel

Publicity

S. Diane Smith, Consultant

Tutorials

Qiang Li, Santa Clara University

At Large

Martin Freeman, Philips Research

John Hennessy, Stanford University

August 15, 1994 — Memorial Auditorium

9:00 - 9:15	Welcome and Opening Remarks John Mashey, General Chair Don Alpert and Alan Jay Smith, Program Co-Chairs	
9:15 - 10:45	Session 1: CPUs—1 Session Chair: Norman P. Jouppi, DEC WRL	
	• An Overview of the 21164 Alpha AXP Microprocessor	1
	John Edmondson, Paul Rubinfeld, Digital Equipment Corp.	
	• The Power2+ Processor	9
	David Shippy, IBM	
	• A 500MHz 32b 0.4um CMOS RISC Processor (Gallop)	19
	Kazumasa Suzuki, NEC Corporation	
10:45 - 11:15	Break	
11:15 - 12:45	Session 2: Multiprocessors and Encryption Session Chair: Howard Sachs, Sun Microsystems	
	• The Alewife CMMU: Addressing the Multiprocessor Communications Gap	31
	John Kubiawicz, MIT	
	• nCube3 Integrated MPP Node Processor	43
	Robert Duzett, nCube	
	• A 100Kbit/sec Single Chip	53
	Modular Exponentiation Processor Holger Orup, Aarhus University, Denmark	
12:45 - 2:15	Lunch	
2:15 - 3:45	Session 3: Networks, Communications Session Chair: Forest Baskett, Silicon Graphics	
	• UAI2110: A Universal GaAs ATM Interface Chip for High Speed Networks	61
	Premysl Vaclavik, Thomas Neuroth GmbH, Austria	
	• A 500 MHz BiCMOS GByte/Second SCI-Link Implementation	69
	Wayne Nation, IBM	
	• The STC104 Asynchronous Packet Switch	77
	Peter Thompson, INMOS Ltd.	
3:45 - 4:30	Break	
4:30 - 5:30	Session 4: CPUs - 2 Session Chair: Don Alpert, Intel Corporation	
	• The New i960 CPU that offers More for Less, the P100	89
	Richard Brunner/Deif Atallah, Intel.	
	• SH-II: A Low Power RISC Micro for Consumer Applications	97
	Shumpei Kawasaki, Hitachi	
5:30 - 7:00	Monday Evening Buffet Dinner	
7:00 - 9:00	Evening Panel Session The Investor (Venture) Community View of What's Hot Moderator: Forest Baskett, Silicon Graphics	
	Panelists:	
	Cliff Friedman, Senior Managing Director, Bear Stearns	
	Stephen Shapiro, Portfolio Manager, Tiger Management	
	Peter Thomas, General Partner, Institutional Venture Partners	

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August 16, 1994 Memorial Auditorium

9:00 - 10:00	Session 5: Chipsets Session Chair: Allen Baum, Apple Computer • 82430NX PCiSet: Companion to the Highest Performance Pentium Processor 105 Patrick Correia, Intel Corporation • A Power PC/PCI Bridge Chip with a Cache and Memory Controller 115 Karl Wang; Motorola, Inc.
10:00 - 10:30	Break
10:30 - 12:30	Session 6: Graphics Session Chair: Ruby Lee, Hewlett Packard • An ASIC for Interactive 3D Graphics 123 Stephanie Winner, Apple Computer Inc. • GLiNT - a 3D Graphics Processor Based on the OpenGL Standard 131 Neil Trevett, 3DLabs • The Smart Frame Buffer Goes Hollywood: 3D and TV 143 Joel McCormack, Digital Equipment Corporation • A Cached VRAM for 3D Graphics 153 Michael Deering, SUN Microsystems
12:30 - 2:00	Lunch
2:00 - 3:30	Session 7: Video Session Chair: Anoop Gupta, Stanford University • Video Compression Processor for H.320-to-Indeo Transcoding 163 Bryan Martin, Integrated Information Technology • A High Performance Programmable Multi-standard Video Compression Chip Set 171 David Still, Array Microsystems Inc. • Multimedia Enhancements for PA-RISC Processors 183 Ruby Lee, Hewlett-Packard
3:30 - 4:00	Break
4:00 - 6:00	Session 8: CPUs - 3 Session Chair: Alan Jay Smith, University of California, Berkeley • PowerPC 604 193 Marvin Denman, Motorola • The Thunder SPARC Processor 201 Bruce Lightner, Metaflow Technologies Inc. • The Superscalar Hardware Architecture of the MC68060 211 Joe Circello, Motorola • A High Performance, Low Power, Pentium Processor Doug Carmean, Lawrence Clark, Robert Rozploch, Intel
	6:00 Closing Remarks

Program Committee Co-Chairs
Donald Alpert, Intel
Alan Jay Smith, UC Berkeley

Program Committee Members
Forest Baskett, Silicon Graphics
Allen Baum, Apple Computer
Anoop Gupta, Stanford University

Keynotes