



Touchstone - A Fresh Approach to Multimedia for the PC

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Presentation Outline

- Touchstone Background
- Chipset Overview
- Sprite Chip
- Tiler Chip
- Compressed Textures
- Advanced Rendering Features

Touchstone Background

- First Implementation of Features in the Talisman Architecture
- Integrated 3D/multimedia chipset for the PC
- Joint development project:
 - Cirrus Logic
 - Fujitsu Microelectronics
 - Microsoft Corporation
 - Samsung Semiconductor
 - Silicon Engineering

Touchstone Goals

- Create a new media solution which addresses key limitations in the PC architecture
 - Memory bandwidth limitations for 3D graphics
 - Advanced 3D rendering features
 - Integration of 2D, 3D, audio and video
 - Enable programmable media accelerators
 - Optimized for DirectX

Product Differentiation

- Integrated Audio, Video, 2D and 3D graphics
 - Simplifies content development & Lowers overall system cost
- 1024x768 24-bit RGB at 72Hz versus 640x480 16-bit RGB at 30Hz
 - Sharper images without banding
 - 72Hz frame rate greatly improves immersive experience
 - Optimized for guaranteed frame rate
- Effective polygon rate of 2M triangles/sec
 - Allows for more complex environments
- Advanced rendering features
 - Provides higher-quality imaging and special effects

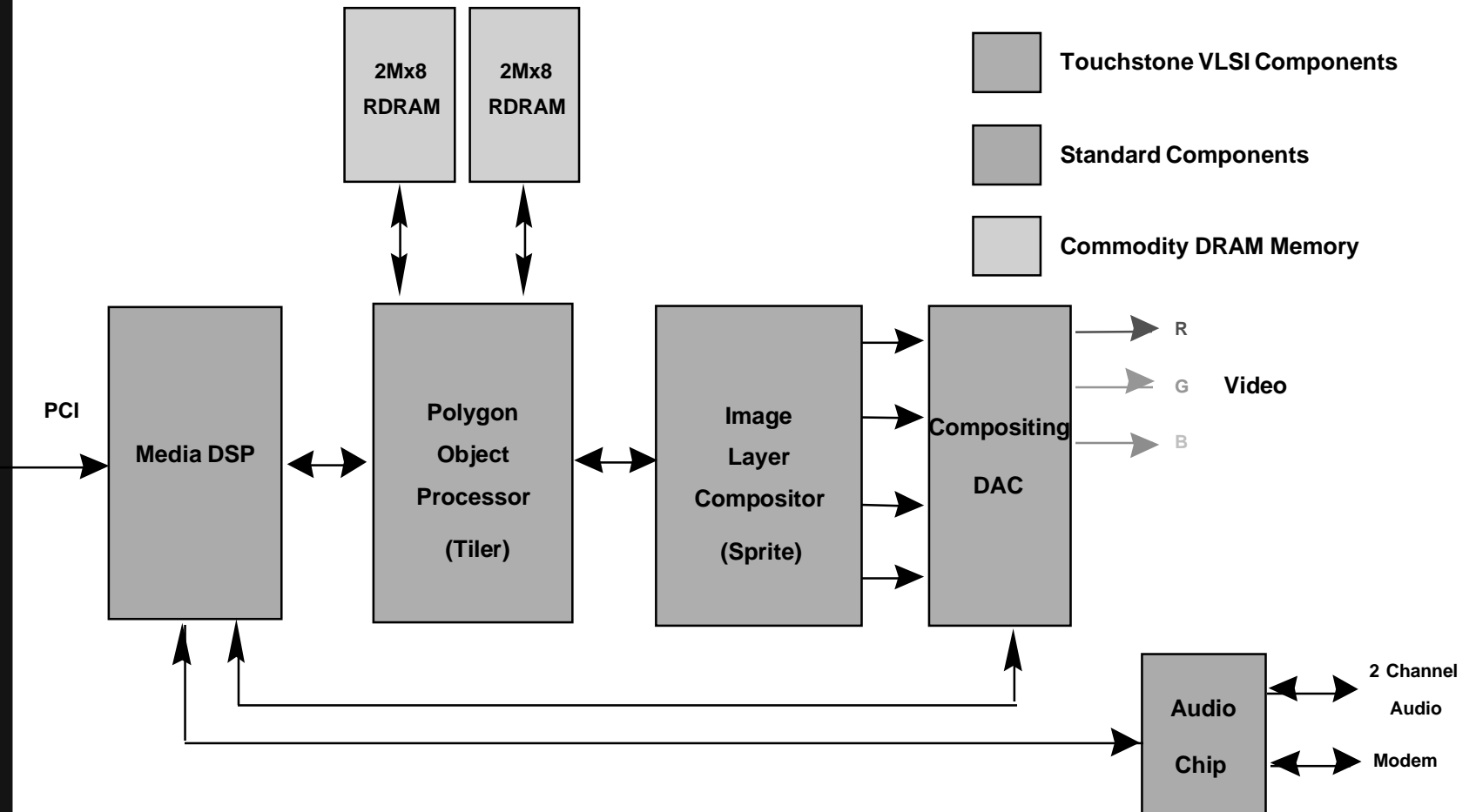
Chipset Overview

- **Tiler & Sprite Chips: Silicon Engineering/Cirrus Logic**
 - Memory Controller
 - 3D Rendering Pipeline
 - Performs GSprite transformation and controls Compositor
- **Media Signal Processor (MSP) - Samsung Semiconductor**
 - Real-Time Kernel, Graphics Control, Geometry, MPEG, Audio
- **Compositing DAC: Fujitsu Microelectronics**
 - Compositing Buffer for GSprites into display image
 - RAMDAC

3D Graphics

- Existing architectures evolved from Mechanical CAD
- Animation achieved through brute force
 - Re-render entire screen at frame rates
- How can we use silicon more efficiently?

Chipset Overview



Key Concepts:

- DirectDraw Surfaces
 - Affine Transform and Composite Surfaces in Display Pipeline.
 - Exploits Temporal Coherency of 3D apps, re-use surfaces
- Compressed Textures and Surfaces
 - Amplifies Memory Capacity and Bandwidth by 10x.
- Chunking
 - Render 32x32 tiles of a surface at a time
 - No Global Z-buffer, or Anti-aliasing buffers needed.

Rendering Pipeline

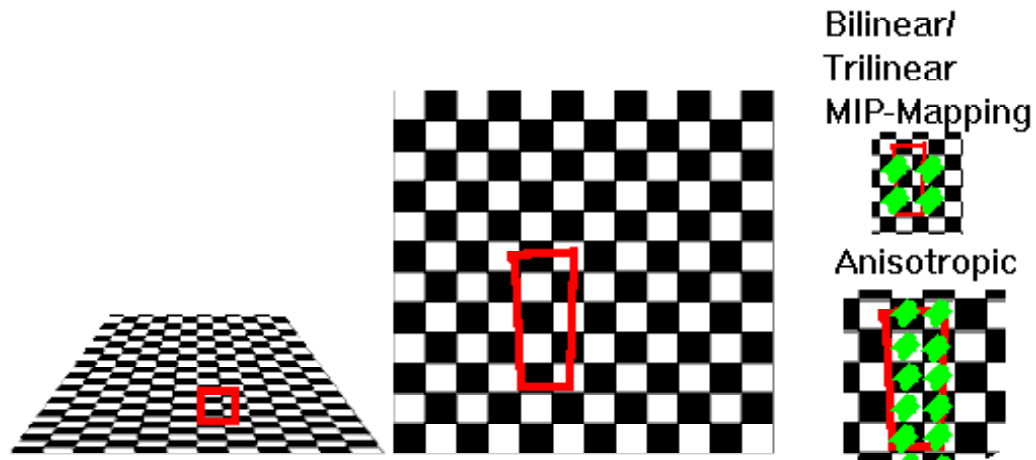
- MSP performs “Geometry Engine” operations
 - Transform, Light, Clip, Setup
 - Separate triangles into bins, depending on viewable area
- Tiler renders DirectDraw Surfaces, one chunk at a time
 - Display list input - pointers to bins needed for each chunk
 - Renders primitives into chunk-sized buffer (32x32)
 - Chunk is compressed and stored in memory

Display Pipeline

- MSP creates a surface display list, in front-to-back order
- Compositing-DAC signals start of display
- Display is composited one band at a time (1344x32)
 - Sprite Chip fetches surfaces, performs affine transform
 - Compositing buffer receives pixels from Sprite Chip, composites one band at a time, then displays completed bands

Advanced Feature: Anisotropic Texture Filtering

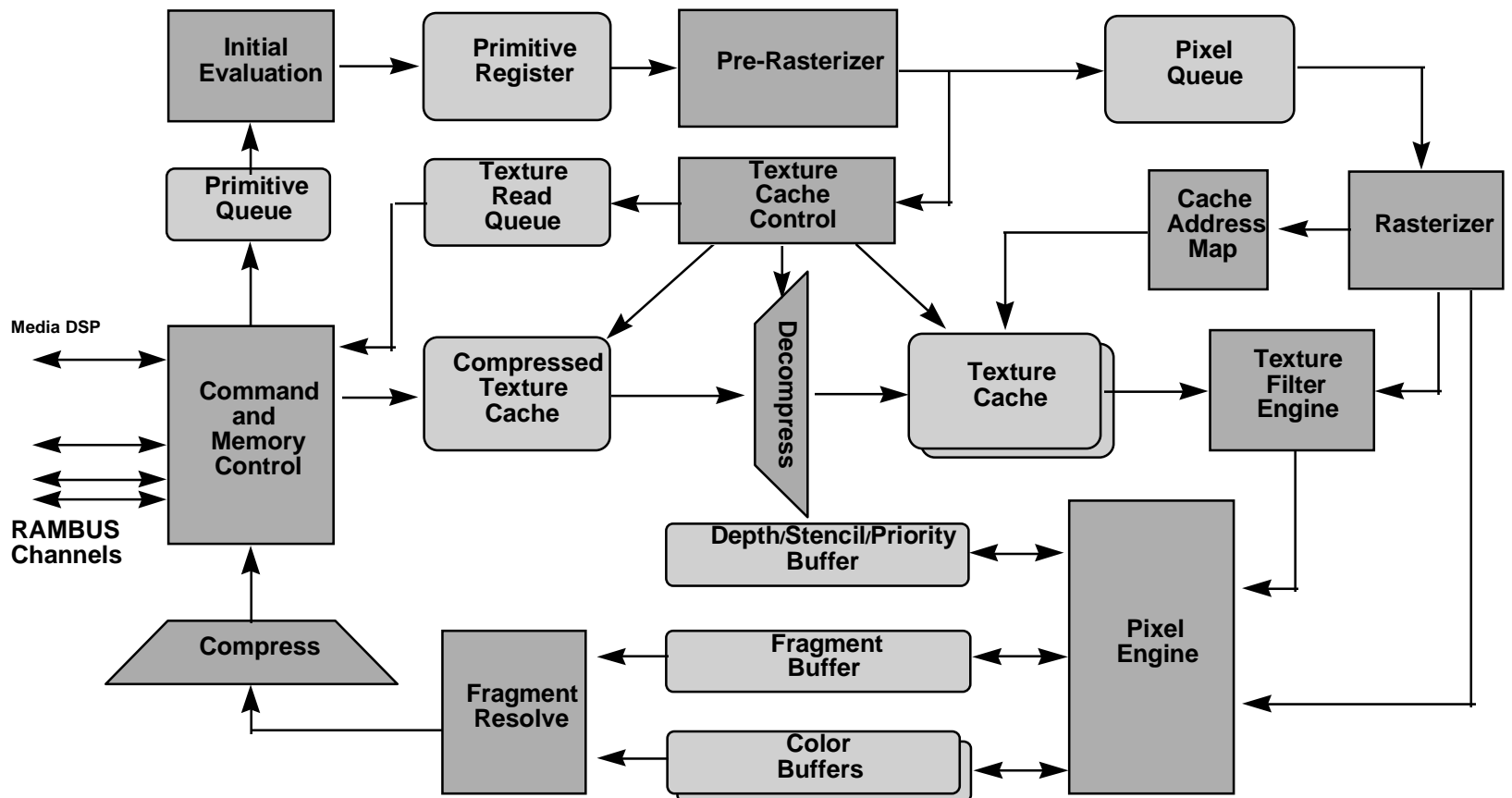
- Provides sharper textures (without temporal artifacts) especially at high angles of perspective



Sprite Chip - Functional Overview

- Fetches DirectDraw Surfaces from memory at display time
- Performs affine transforms on DirectDraw Surfaces
- Filtering Modes: Point Sampled, Bilinear, Bicubic
- Composites one display band at a time, rendering front to back and writing results to Compositing Buffer
- Composites Pixels at 320Mpixels/sec (1.28GBytes/sec)

Tiler Chip - Block Diagram



Tiler Chip - Functional Overview

- Chunk-based rendering pipe
 - Display List Processor
 - Clip triangle to Chunk, and calculate starting point's attributes
 - Interpolate coordinates, colors and texture coefficients - Calculate coverage mask
 - Calculate texture coordinates, lookup samples and filter
 - Per-Pixel operations: Z-buffering, Anti-aliasing, Transparency, stencil, etc
 - After entire chunk is rendered, it is compressed and written to memory

Compressed Textures: Challenges

- Texture mapping accesses data randomly
 - Most compression methods need to read most of image to decompress one pixel
 - How do you find the random data in a compressed image?
- Long Latency Between Address Generation and Uncompressed Data Available.
 - Uncompressed 3-D address Needs to be mapped to linear, compressed address
 - Data Fetch
 - Data Decompress

Challenge 1: Not Fetching Most of Image.

- Solution: Use Jpeg-like 8x8 compressed blocks.
- Key difference: DC components not differentially encoded.
- Cache 8x8 blocks uncompressed for re-use.

Challenge 2: Random Access.

- Solution: List of pointers to Compressed blocks kept in linear Memory
- Compressed data stored in Linked-list memory: Simplifies memory allocation.
- Caching of sections of the pointer list, and linked - list elements (128-byte MAUs) in compressed cache increases effective cache size by 10x.

Challenge3: High Latency.

- Solution 1 (Sprite Chip): Two Rasterizers.
 - Surface edge equations are fed into Pre-Rasterizer and FIFO to Post-rasterizer.
 - Pre-Rasterizer calculates addresses, forcing compressed cache hits/misses early.
 - Post Rasterizer calculates same address sequence later, forcing uncompressed cache hits/misses.
 - Time between Pre-and post rasterization used to fetch and uncompress blocks.

Challenge3: High Latency.

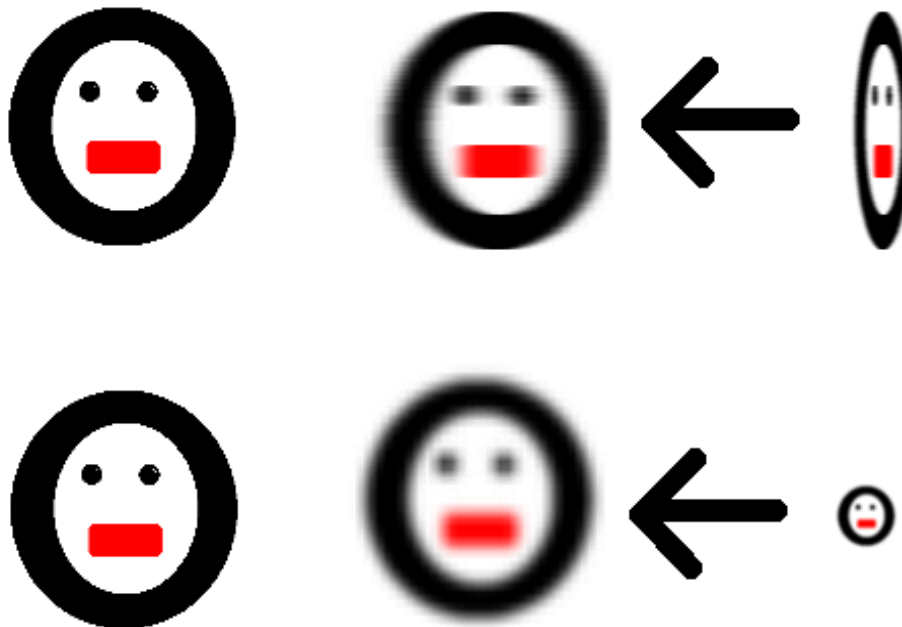
- Solution 2: (Tiler Chip): One Rasterizer, Big texel address FIFO.
 - Rasterizer calculates addresses, forcing compressed cache hits/misses early.
 - Rasterizer places addresses in Pixel FIFO
 - Addresses are applied to the uncompressed cache later, after blocks have been fetched and uncompressed.

Advanced Rendering Features:

- Anisotropic Texture Filtering
- Shadows
- Transparency
- Anti-Aliasing
- Motion Blur
- Depth-of-Field Effects

Advanced Features: Motion Blur and Depth-of-Field

- Render Object in separate GSprite, shrink in one or both dimensions. Expand to normal size during display.



Functionality and Performance

- Single PCI board with audio, video, 2D and 3D graphics
- High-resolution display 1344x1024 @ 75Hz
- 24-bit true color for all resolutions
- Rendering rate of 40M pixels/sec *with anisotropic filtering and Z-buffered anti-aliasing*
- Image compositing at 320M pixels/sec
- Equivalent to 2M polygons/sec
- Advanced rendering features - subpixel-filtered anti-aliasing, translucent surfaces, shadows, blur, fog, etc

Conclusions

- >120x overall performance improvement:
 - >4x performance improvement through Spriting
 - 10x memory capacity and bandwidth improvement through Compression
 - 3x memory bandwidth improvement through Chunking
- Allows RE2-level performance, image quality, features at PC price points