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HOT-CHIPS SYMPOSIUM: Hot off the Drawing Board

Business/Technology Editors

PALO ALTO, Calif. --June 15, 2001——What do you do when you've developed the hottest, baddest, fastest chip on the planet? You lobby to present your work at the prestigious Hot Chips Conference at Stanford University. The conference, originally sponsored by John Hennessey, President of Stanford University, has been attracting the finest microelectronic innovations for more than a decade. It has served as a forum for the earliest development of RISC architectures, RAID storage, CMOS imaging, ultra low-power processors and non-conventional processors (e.g. quantum). This year's conference, Hot Chips 13 (www.hotchips.org) is coming around again, on Aug. 19-21, 2001 at Stanford University.

Hot Chips focuses on real products and real technology, and lets developers and engineers from around the world check out the next generation of microprocessors, network processors and storage technology.

Over three days, the conference features tutorials and keynote speakers in addition to technical presentations. Timely tutorials will focus on third generation wireless technology and mixed-signal IC design. The three-hour wireless tutorial will discuss opportunities offered by the progress in semiconductor technologies, an exploration of the needs of future wireless systems, an overview of the different solutions, and clear metrics in how to evaluate and compare options. The afternoon Mixed Signal tutorial will address design methodology for high-end analog, including a beginners overview of why analog is not like digital design: why it's weird, where it's weird, how designers cope.

Continuing the trend that has included prominent CEOs, keynoters this year are Atiq Raza and Mark Dean. Prior to founding **Raza Foundries**, Atiq Raza was president and COO of **AMD**, where he directed the development of the K6 processor and laid the foundation for the Athlon processor lines which has restored AMD's competitiveness with Intel. Mark Dean, was instrumental in the development of the bus control systems used in modern microcomputer systems. His inventions paved the way for the growth in the Information Technology industry by allowing the use of plug-in subsystems

and peripherals like disk drives, video gear, speakers, and scanners. Dr. Dean, an **IBM** Fellow and VP of Systems Research, will discuss Trends Impacting Computing Systems Design and the IT Industry.

Presentations come from a broad spectrum of industry: **SGI**, **IBM**, **Intel**, **Qualcomm**, **Hitachi**, **Agere Systems**, **Toshiba**, and **ARM**, and hot startups with innovative ideas such as **Tensilica**, **nBand Communications**, **Mellanox Technologies**, **Accelerant networks**, **Velio Communications**, **Nishan Systems**, **Alpine Microsystems** and **DataPlay**. Leading edge research from **MIT**, **The Kirchoff Institute for Physics** and the **Univ**. **of Illinois** will also be presented at the conference. The chips discussed range from the latest superscalar microprocessors, to network chips, to graphics controllers and next generation storage devices.

DataPlay will introduce a new technology for information distribution. A 32mm optical disc can be recorded (in situ) with up to 500 MB of downloaded data and containing several hundred MB of prerecorded data in a low cost embossed form somewhat akin to a DVD or CD. Selective access to the disc's content makes possible unique encryption and conditional access keys that insure viable content protection methods. The 32 mm discs are played and recorded on the DataPlay Micro Optical Engine, which is the smallest optical recorder/player ever developed. The heart of the device also integrates the most powerful ECC scheme ever commercialized in this field. The engine is also the first example of an optical drive that uses a tilting rotary actuator that permits rapid data access in a simple mechanism. All this is enabled by the smallest most integrated optical pick up head ever developed, weighing only a few grams and rides on the end of the rotary actuator. These, and other innovations, result in a product that uses a fraction of a watt in typical applications. **DataPlay** and it's partners (**Sonicblue**, **Creative Labs**, **Toshiba**, **Samsung**, **Olympus**) will begin to introduce the technology to the market this fall with music players, digital cameras and other portable digital consumer products.

Agere Systems will present its Fast Pattern and a Routing Switch Processor, around which devices like firewalls, multi-protocol switches and routers can be constructed. The product family represents an order of magnitude improvement in technology for intelligent communication equipment that extends into the 10 Gbit/sec realm and beyond.

Silicon Graphics will disclose details of the newest member of the MIPS architecture, the 4-way dynamic super-scalar processor R18000 Superscalar Microprocessor. The R18000 will extend the "distributed shared memory" features of **SGI's** scalable 64 bit MIPS/IRIX architecture, improves cache and memory performance with a 3-level cache hierarchy, a new dual-path source-synchronous system interface with six times the peak bandwidth of the R14000 system bus and has two floating-point execution units that double the peak FLOPS rate of the R14000.

The **IBM Server Group** will describe the POWER4 chip: a systems design for high reliability. The chip is targeted for frequencies over 1 GHz, contains two independent out-of-order processor cores, each with eight execution units, a shared L2 and L3 directory and all of the logic needed to from large symmetric multiprocessor systems. The chip, containing over 170 million transistors is fabricated using IBM's 0.18 um CMOS SOI technology with 7 layer copper metalization. More than 200 instructions can be in various stages of execution.

Another IBM division, **IBM Microelectronics**, will present a custom designed, PowerPC derivative processor targeted at the video game console market. The Gekko processor provides general-purpose processing performance exceeding 1000 DMIPS. The ISA extensions support increased floating-point throughput, streaming data for models and graphics, and data compression. The presentation will identify the design objectives, describe the graphics-specific features, and summarize the performance of the Gekko chip.

Intel will make three presentations describing the Pentium 4, the Itanium Processor and the 870 family of Enterprise chipsets. The 870 chipsets supports both Intel's latest Itanium Processor Family and the IA32 Intel Xeon processors. It is highly scalable, supports 1 to 16 coherent processors and features robust RAS features including multi-pathing, node hot plug, static and dynamic partitioning. It also supports a flexible memory organization and a number of different I/O interfaces and standards. The Pentium 4 Processor presentation will focus on the main features and functions of the Pentium 4 processor micro-architecture. The front end of the machine, includes its new form of instruction cache called the Execution Trace Cache. The out-of-order execution engine, including the extremely low latency double-pumped ALU

that runs at more than 3.4 Ghz is described. The memory subsystem includes the very low latency L1 data cache that is accessed in just two clock cycles. Key performance characteristics for this processor are compared to the Pentium III processor.

Nishan Systems will present a High Performance Storage Network over an IP Switch Engine for Local and Storage Area Networks. By applying the networking paradigm to storage devices, Storage Area Networks (SAN) enable increased connectivity and bandwidth, sharing of resources and configuration flexibility. The basic premise of a SAN is to replace the current "point-to-point" infrastructure of server to storage communications with one that allows "any-to-any" communications. In its simplest form, a SAN provides LAN-like connectivity, scalability, and availability to enterprise storage resources.

ARM presents its ARM10 Family of Advanced Microprocessor Cores. The family includes the ARM1020E and the ARM1022E cached cores, the VFP10 floating point coprocessor and the ETM10 embedded trace macro-cell. The ARM1020E core includes DSP instruction set extensions, on-chip debugging capabilities, dual 32k caches and full MMU support. In addition dual 64-bit bus interfaces support multi-layer bus architectures. The VFP10 is a tightly coupled vector floating point coprocessor that delivers 600 MFLOPS for 3D graphics, MPEG-4 and real time control systems. Key features of the ARM1020E include: a six stage scalar pipe; power efficient branch prediction with support for branch folding; non-blocking, hit-under-miss caches; and various levels of power-down, the most interesting of which uses a hardware isolation layer around the caches. This allows the power to the rest of the system to be removed while the caches remain powered at a reduced voltage, thus retaining cache state for faster restarts.

Accelerant Networks will present a revolutionary communications transceiver that utilizes many innovative features to move data at 5 Gb/s over traditional backplane interconnects. Combining 2.5GHz multilevel Analog Signaling utilizing a unique encoding scheme, dynamic equalization and inter-channel communications the chip has been implemented in 0.25 um COMS technology.

PMC-Sierra PMC-Sierra will present its 2.5 Tbit/s single-stage, centrally arbitrated switch core, that can interconnect up to 1024 linecards operating at 2.5 Gbit/s, 256 linecards operating at 10 Gbit/s, or 64 linecards operating at 40 Gbit/s. The presentation will describe the key elements of building high capacity switch core systems including detailed discussions of the LCS (Linecard to Switch) protocol, the Crossbar interchanger (how it provides more ports per crossbar chip with the same number of I/Os), and why strict priorities are needed for designing pipelined and redundant schedulers.

IBM Almaden Research Center will present the Microdrive: high capacity storage for the handheld revolution. The Microdrive offers a unique combination of the maximum capacity available (1 GB) and high performance. It uses a single 27.4 mm glass substrate disk and two GMR (giant magnetoresistive) heads operating at an areal density of 15 Gb/sq. inch. The drive’s electronics uses surface laminar circuit (SLC) technology using only one sixth the area of a typical 2.5 inch disk drive. The entire drive is built in a CompactFlash (CF) type 2 form factor. More than 16 hours of MP3 music (128 kb/s) or more than 2 hours of MPEG-4 video (1 Mb/s) can be stored. The drive offers sustained transfer rates of 20-33 Mb/s. The drive achieves the highest shock resistance rating of any disk drive.

Hot Chips began in 1989 as the brainchild of Bob Stewart, a former Governing board member for IEEE Computer Society. His idea was to provide a forum oriented towards what was happening in Silicon Valley.

"We thought a conference on 'Hot Chips' should be affordable and related to real world chips rather than concept related conferences," Stewart said.

Hot Chips has been a significant forum for chip development in Silicon Valley with most of the leading chip makers participating.

"With the dollar value of these products approaching a trillion dollars, the contribution to the user community has been very great indeed," Stewart continued. He added that the 900-1,000 attendees have traditionally drawn from the best and brightest computer engineers and architects.

"The conference is inexpensive, geared toward the real engineering community, and provides access to late-breaking work. Both the presenters and the attendees are an amazing group of the best cutting-edge people in Silicon Valley," said Dr. Forest Baskett, past program chair and venture capitalist.

"The conference is a forum where people get to take a look at the latest processors and chips in a relaxed atmosphere on the university campus and to network with colleagues. It is geared towards practicing engineers, consultants and academia," said Pentium architect Donald Alpert of Intel.

Past Hot Chip conferences featured the 486 and gave first glimpses of the Pentium. This year, in addition to the latest developments in microprocessor architecture and embedded solutions, integrated switch, network and communications chips will share center stage with the latest advances in data storage technologies.

"Most successful chips fill a very specific need," said UC Berkeley professor Alan Jay Smith, a long time attendee and a past Program Chair. "In an environment where massive chips are competing for the same market, it is important to be able to meet the designer and see what is under development."

Alpert agrees that the real benefit of attending Hot Chips is gaining the engineering and technical perspective on upcoming chips. Hearing about technically innovative, emerging applications and processors, their problems, solutions and business impacts, and the future of the technology presented are the best reasons for attending Hot Chips.

Registration fees for the Hot Chips conference are $75 for students and $200 for IEEE/ACM members and $275 for non-members who register by July 28. Registration includes conference proceedings, a CDROM of the presentation, on-campus parking and all meals, alcoholic beverages and snacks. The conference is open to engineers, technology consultants, media, academia, venture capitalists, and high tech marketers who are interested in keeping up with the hottest chips in Silicon Valley.

For more information, please check out the web site at www.hotchips.org.

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