


HOT CHIPS 23

ADVANCE PROGRAM HOT CHIPS 23

A Symposium on High-Performance Chips
August 17-19, 2011, Memorial Auditorium,
Stanford University, Palo Alto, California

HOT CHIPS brings together designers and architects of high-performance chips, software, and systems. Presentations focus on up-to-the-minute real developments. This symposium is the primary forum for engineers and researchers to highlight their leading-edge designs. Three full days of tutorials and technical sessions will keep you on top of the industry. Register for Early Registration rates before Aug.5

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Wed. Aug. 17	Morning Tutorial	Package-Scale Power Management	UC Berkeley
	Afternoon Tutorial	The Open Compute Project	FaceBook
Thursday August 18	ManyCore	<ul style="list-style-type: none"> Cavium OCTEON II CN6880 Multi-Core MIPS64 Processor The IBM Blue Gene/Q Compute chip with SIMD Floating-Point Unit The Highly-Efficient Architecture of the Godson-Core Processor 	Cavium IBM ICT, Chinese Academy of Science
	Security	<ul style="list-style-type: none"> Universal Programmatic Access to High Quality Random Numbers The TILE-Gx ManyCore Processor: Hardware Acceleration Interfaces and Mechanisms Building a 40Gbps, Next-Generation Virtualized Security Processor 	Intel Tilera Cavium
	Keynote 1 ARM Processor Evolution: Bringing High Performance to Mobile Devices	Simon Segars, VP	ARM
	Memory & FPGA	<ul style="list-style-type: none"> The Bandwidth Engine: Serial Memory Chip Breaks 2 Billion Accesses/sec Hybrid Memory Cube: a Re-Architected DRAM Subsystem The Xilinx Zynq Embedded Processing Platform 	Mosys Micron Xilinx
	DSP	<ul style="list-style-type: none"> The XMOS Architecture and the XS1Chips The Worlds' Fastest DSP Core: Breaking the 100 GMAC/s Barrier 	XMOS Tensilica
	Miscellaneous	<ul style="list-style-type: none"> Rethinking Algorithms: Communication-Avoiding Algorithms Electrons, Photons, Phonons, Waves, Bits, and ID: Microsoft Kinect 	UC Berkeley Microsoft
	Panel Ecosystem Wars: It's Not Just About Architecture		
Friday August 19	Networking	<ul style="list-style-type: none"> A Low-Power, High-Density 10GBASE-T Ethernet Transceiver A One Billion Packet per Second Frame Processing Pipeline Sereno: A 2nd-Generation, Virtualized Network Interface Controller 	Aquantia Fulcrum Cisco
	Server	<ul style="list-style-type: none"> Building Data Center Servers Using "Cell Phone" Chips Poulson: An 8-Core, 32nm Next-Generation Intel Itanium Processor T4: A Highly-Threaded, Server-on-a-Chip with Native Support for Heterogenous Computing 	SeaMicro Intel Oracle
	Keynote 2 Challenges of Building Personal Robots	Steve Cousins	Willow Garage
	Video	<ul style="list-style-type: none"> 1TOPS/W Software Programmable Media Processor The Intel Quick Sync Video Technology in the 2nd-Generation Intel Core Processor Family 	Movidius Intel
	Desktop CPUs	<ul style="list-style-type: none"> Second-Generation Intel Core MicroArchitecture Power Management of the 2nd-Generation Intel Core MicroArchitecture AMD's Llano Fusion APU The Performance- and Power-Efficient Bulldozer x86-64 Server for Workstation and Desktop Processors 	Intel Intel AMD AMD
	Please visit us on the web: http://www.hotchips.org or drop us a line via Email: info2011@hotchips.org	 IEEE	



This is a preliminary program; changes may occur. For the most up-to-the-minute details, please visit our web site where you can also check out HOT Interconnects (another HOT Symposium being held following HOT CHIPS)



A Symposium of the Technical Committee on Microprocessors and Microcomputers
of the IEEE Computer Society and the Solid State Circuits Society
in cooperation with the Association of Computing Machinery