Status and Prospect for MRAM Technology

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Nonvolatile Memory Seminar

Hot Chips Conference

August 22, 2010

Memorial Auditorium

Stanford University

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Agenda

- Current status of MRAM products
- MRAM features
- Current MRAM product operation
- Recent advancement in MRAM technology
- Prospect for MRAM

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Everspin Introduction

- **Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor**
- **The leading developer and manufacturer of integrated magnetic products**
  - Industry-first MRAM supplier since June 2006
  - Embedded MRAM systems
  - Integrated magnetic sensors
- **Current MRAM products**
  - Parallel interface products ranging from 256k-16Mb
    - Infinite endurance, >20 year data retention, 35 ns read & write speed
  - Serial interface products ranging from 256kb-1Mb
    - 40 MHz SPI interface, No write delay, infinite endurance

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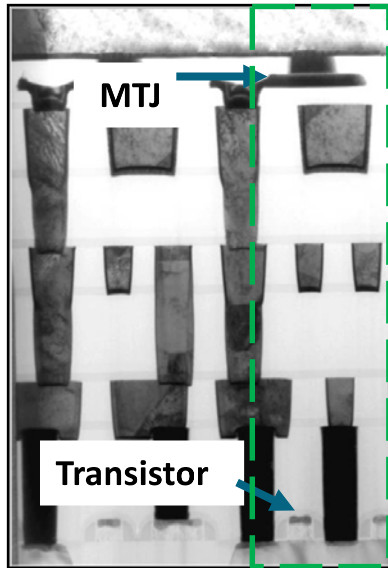
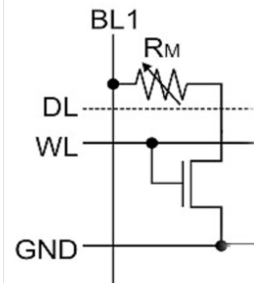
Everspin MRAM Technology



Cross-sectional view



Circuit

- Simple 1 transistor + 1 MTJ memory cell
- Data stored in magnetic polarization, not charge
- State of bit detected as change in resistance
- Always non-volatile
- Non-destructive read, unlimited endurance
- Leverage CMOS semiconductor ecosystem
- Everspin - “Electron spin is forever”

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Everspin MRAM Advantages

Parameter	Capability
Non-volatile capability	• Data retention >20 years
Performance	• Symmetric read/write – 35ns
Endurance	• Unlimited cycling endurance
CMOS integration	• Easily integrates in manufacturing back-end • Compatible with embedded designs • No impact on CMOS device performance
Temperature range, reliability	• -40ºC < T < 150ºC operation demonstrated • Intrinsic reliability > 20 years lifetime at 125ºC
Soft error immunity	• MRAM cell radiation tolerant • Soft error rate from alpha radiation too low to measure (<0.1 FIT/Mb)
Environmentally friendly	• No battery, RoHS compliant, low power

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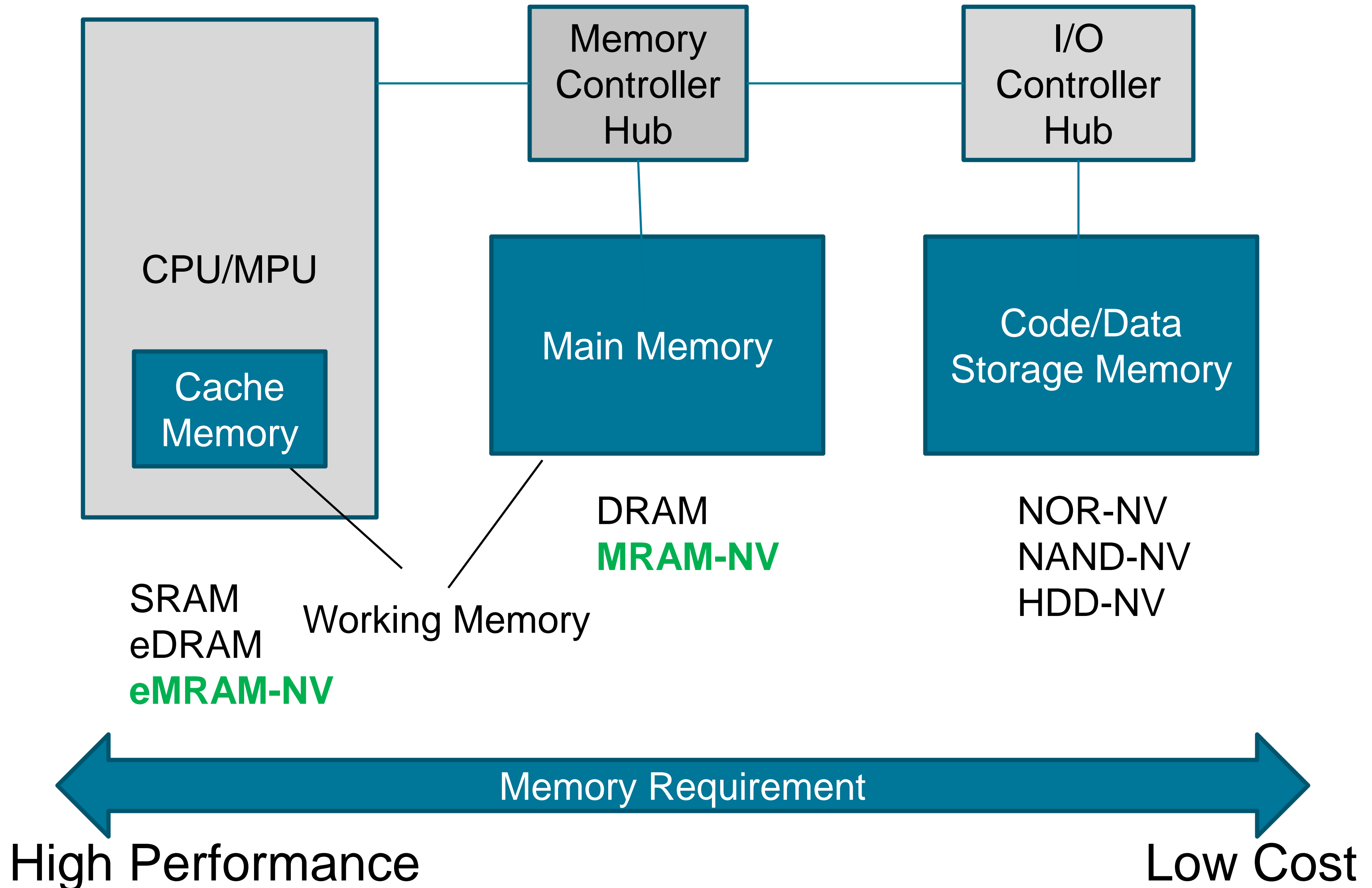
Memory System Hierarchy



Memory Capacity vs. Cycle Time

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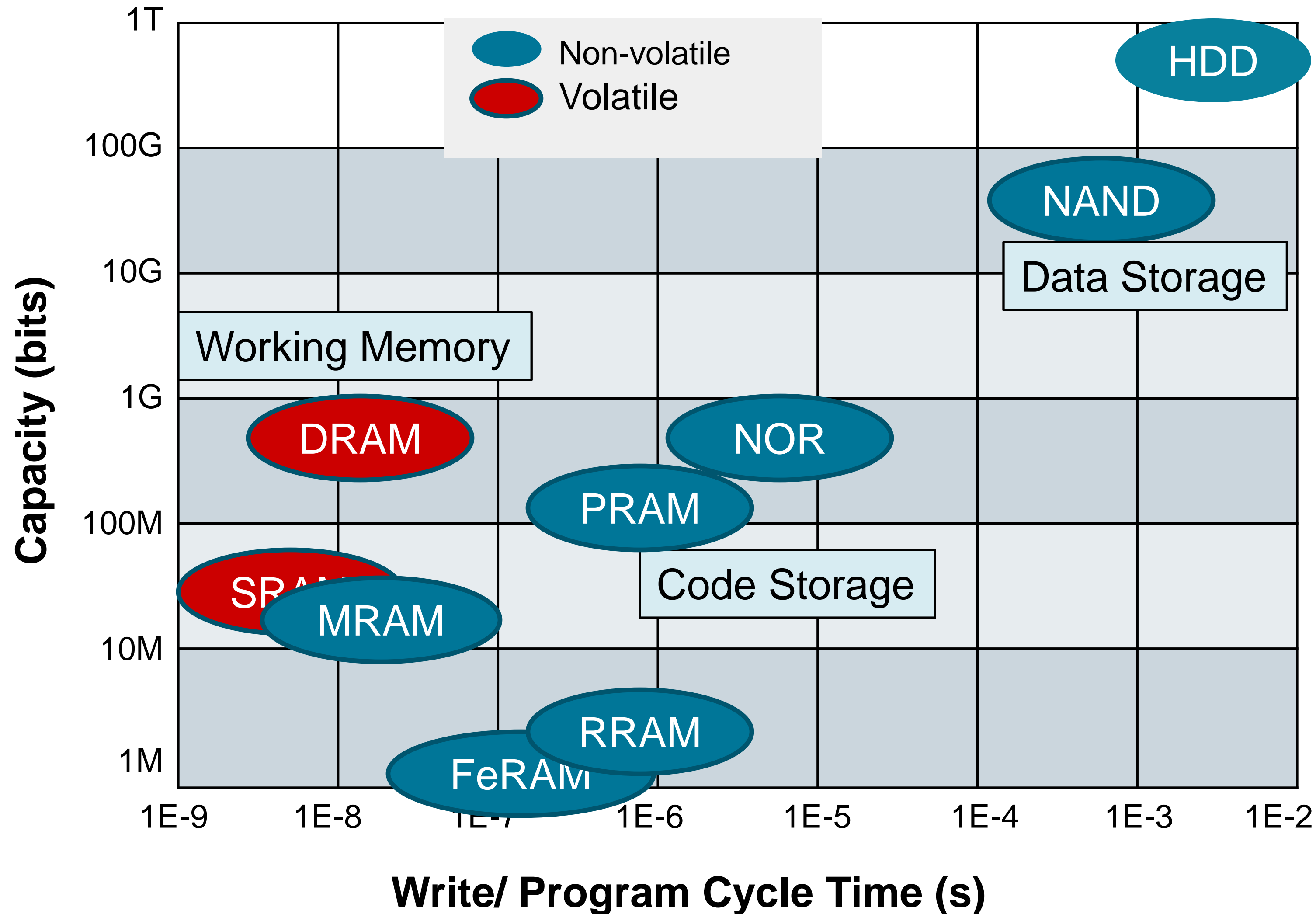

Memory Endurance vs. Cycle Time

SRAM
MRAM
DRAM
HDD
1E15
Working Memory
Data Storage
FeRAM
1E12
1E9
Non-volatile
Volatile
1E6
PRAM
NOR
RRAM
1E3
NAND
Code Storage
1E0
1E-9
1E-8
1E-7
1E-6
1E-5
1E-4
1E-3
1E-2

Endurance (Cycles)

Write/ Program Cycle Time (s)

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MRAM Writes and Reads

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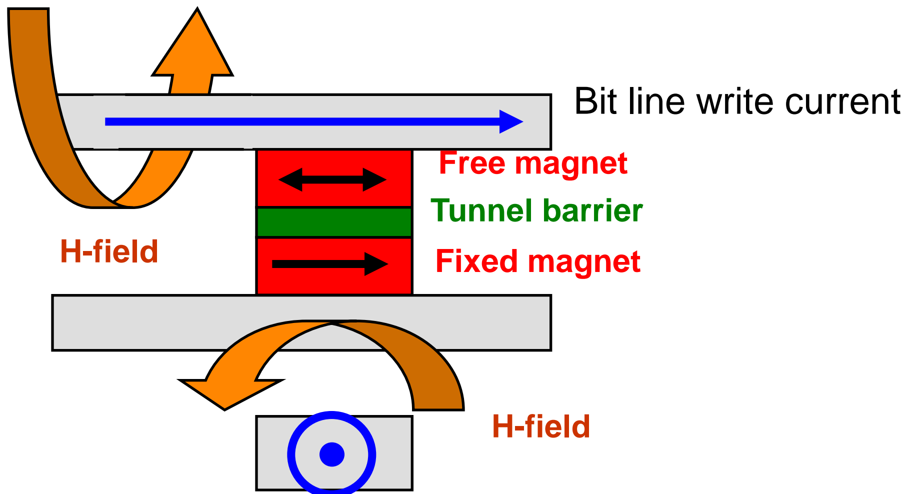
Toggle-MRAM in production



- Cross-point architecture
- Current along bit line and digit line to switch at intersection

- Write Current Flows Down Write Line 1 & 2
- Magnetic Tunnel Junction (MTJ) At Cross-Point Is Polarized
- Polarization State Is Read By Selecting Pass Transistor to Sense Resistance of Specific MTJ

Toggle MRAM Bit Cell

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Program Line 2

Tri-layer is called a synthetic antiferromagnet, or SAF

Free Tri - Layer

Ferromagnetic layer

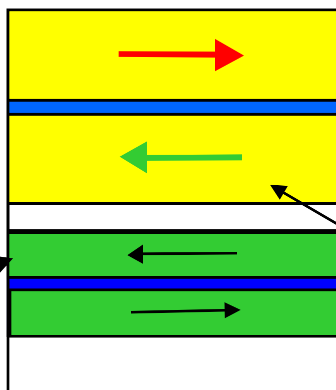
Coupling Layer

Ferromagnetic layer

Tunnel Barrier

Pinned Ferromagnetic

Pinning Layer



Program Line 1

Only the orientation of the bottom layer of the free SAF affects the tunneling and therefore the resistance of the bit.

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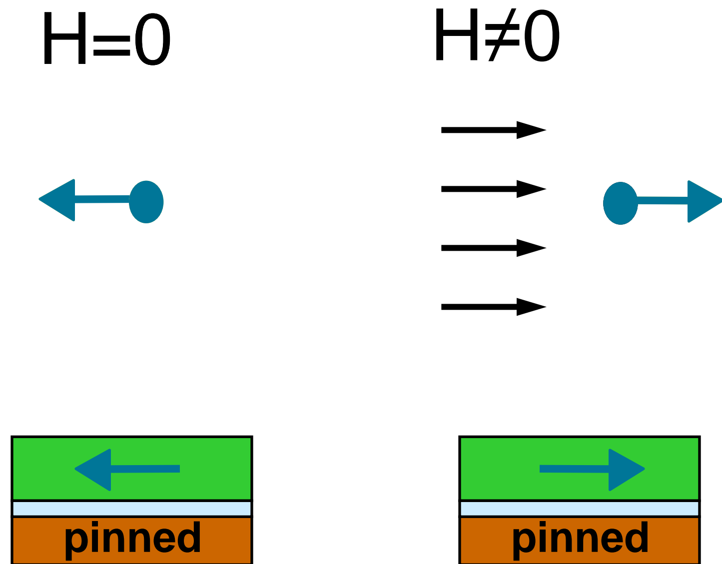
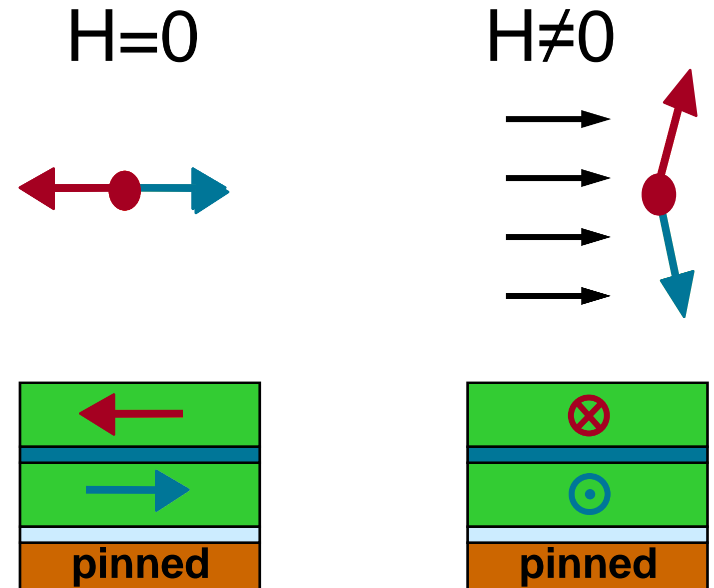
Free Layer Field Response

Conventional MRAM
Single Layer



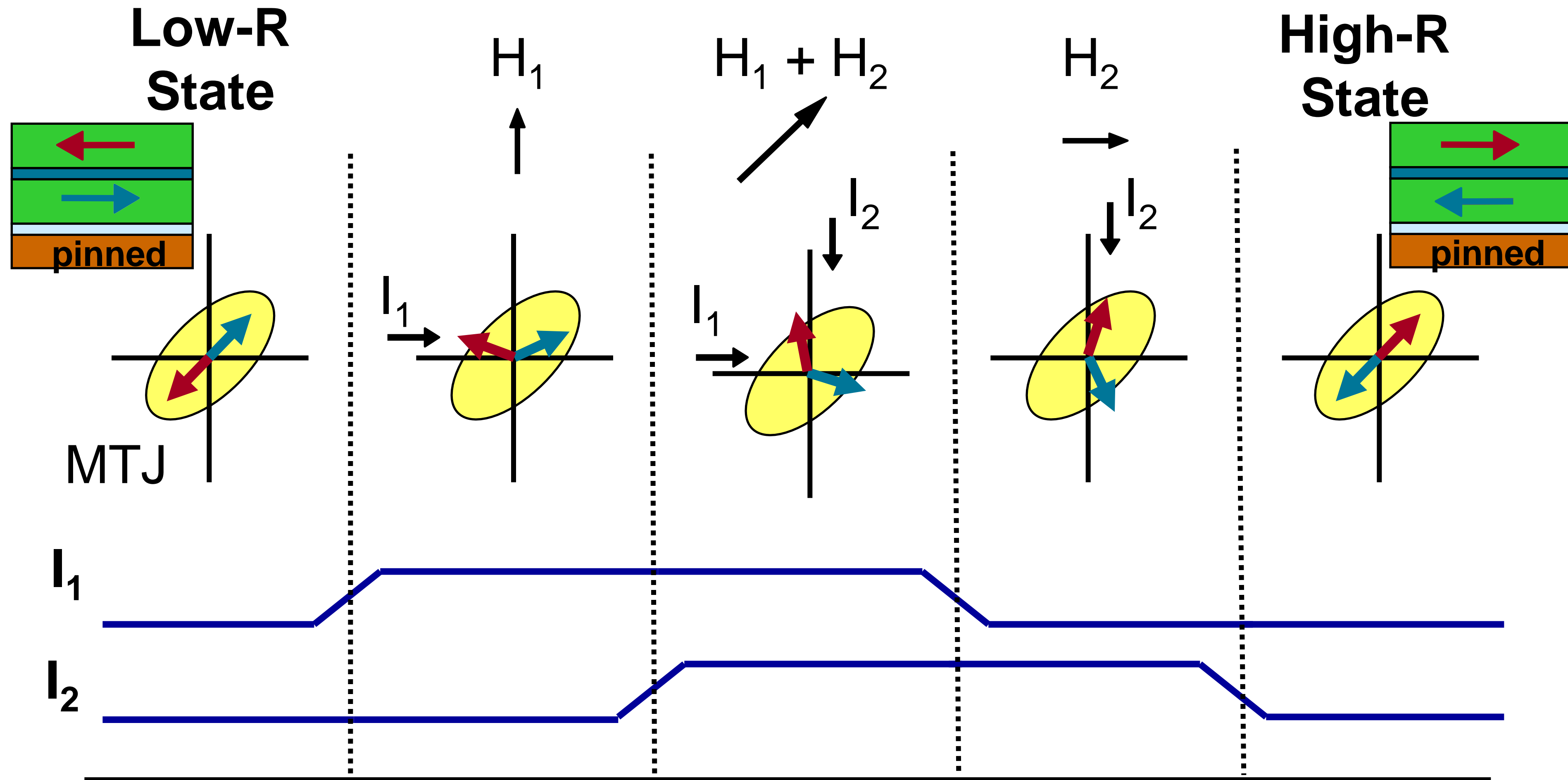
Aligns with applied field

Toggle MRAM
Coupled Trilayer



Rotates perpendicular to applied field

Toggle Write Operation



Advantages: Eliminates disturb - Large operating window

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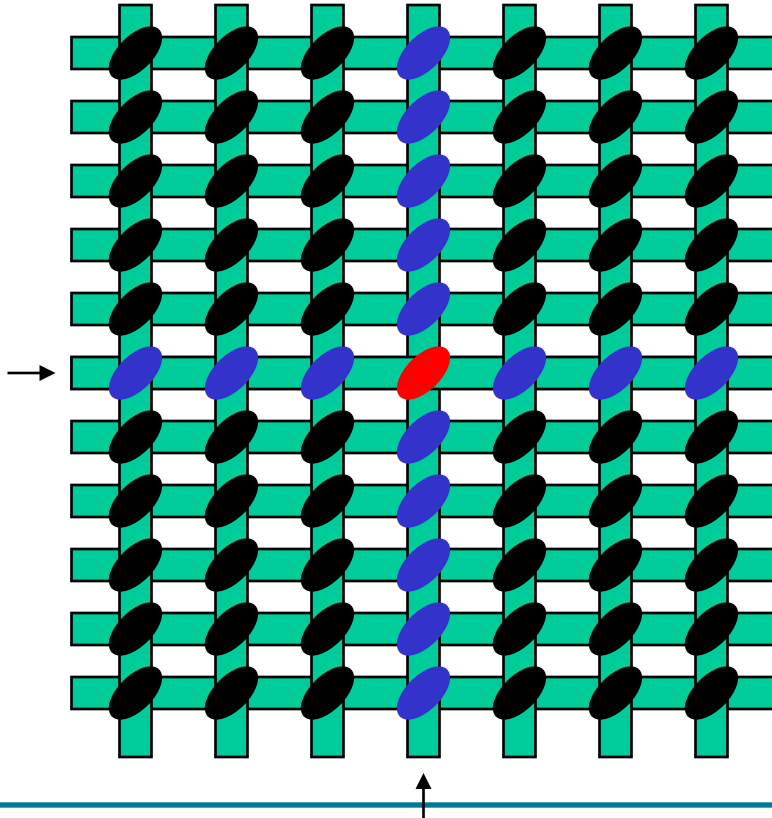
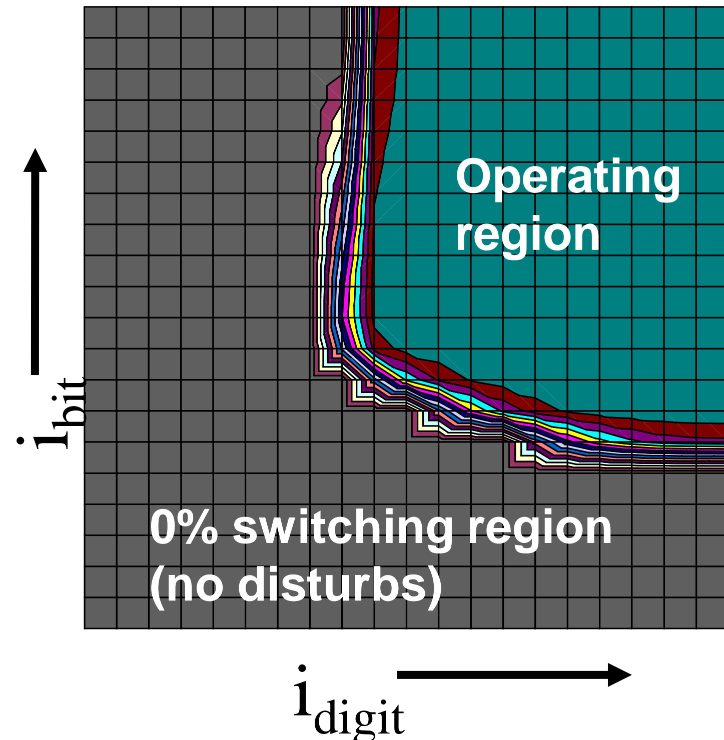
Toggle-Bit Selection

- No ½-select bit disturb
- All bits along ½-selected current lines have increased energy barrier during programming
- Single write line can not switch bits



4Mb, March6N Toggle Map



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MRAM Storage Concept

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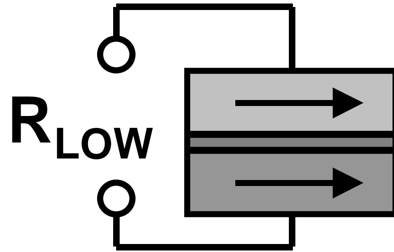
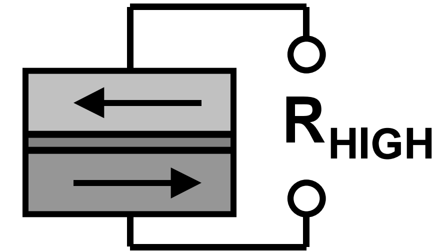
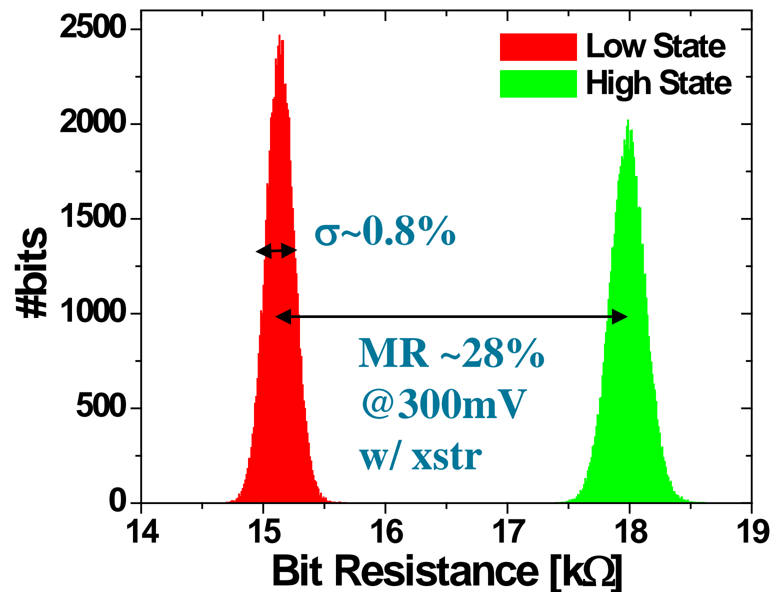


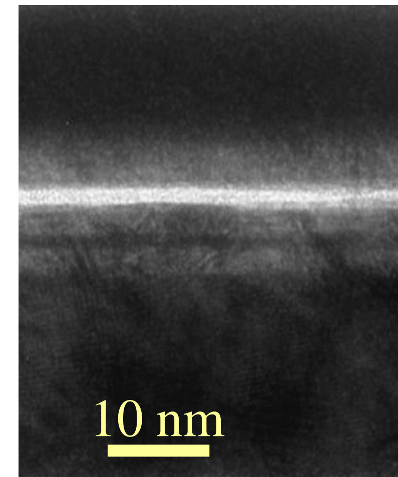
Free Layer
Tunnel Barrier
Fixed Layer



Parallel = Low Resistance

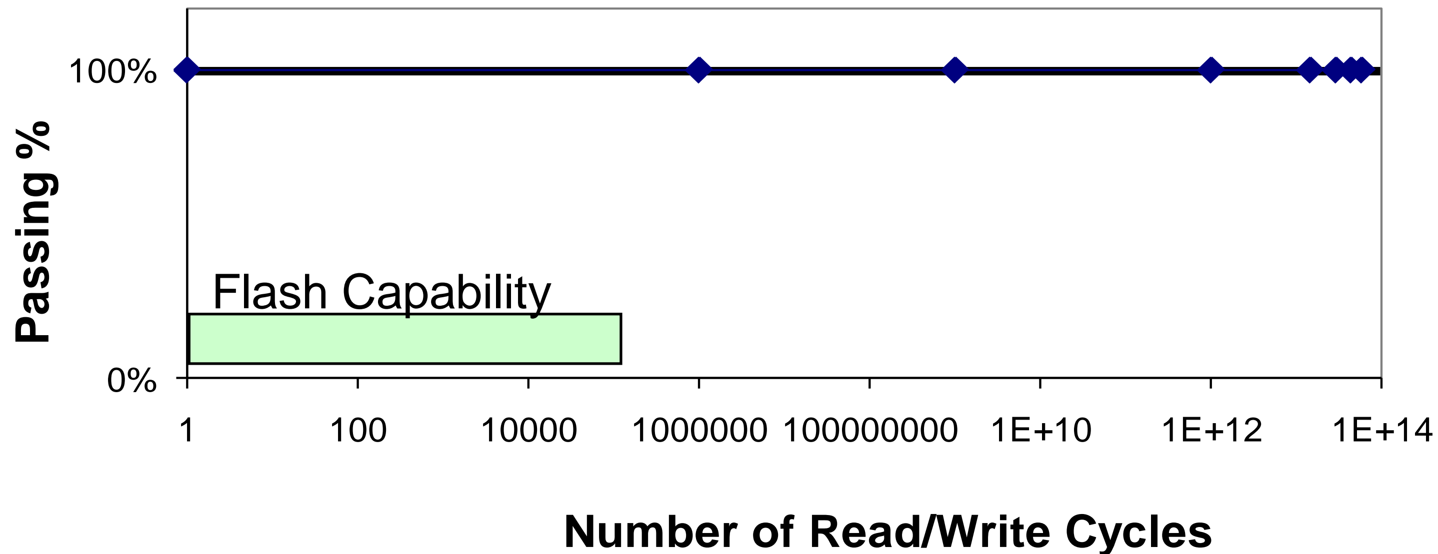
Anti-Parallel = High Resistance





NiFe/AlOx/NiFe

MRAM: Unlimited Read/Write Endurance



- MRAM Endurance Tested to 58 Trillion Cycles with No Change in Critical Parameters.
- Data from >2800 bits from 900 devices
- 8 orders of magnitude more cycles than current Flash technology
- No known failure modes are seen or expected

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MRAM bit switching

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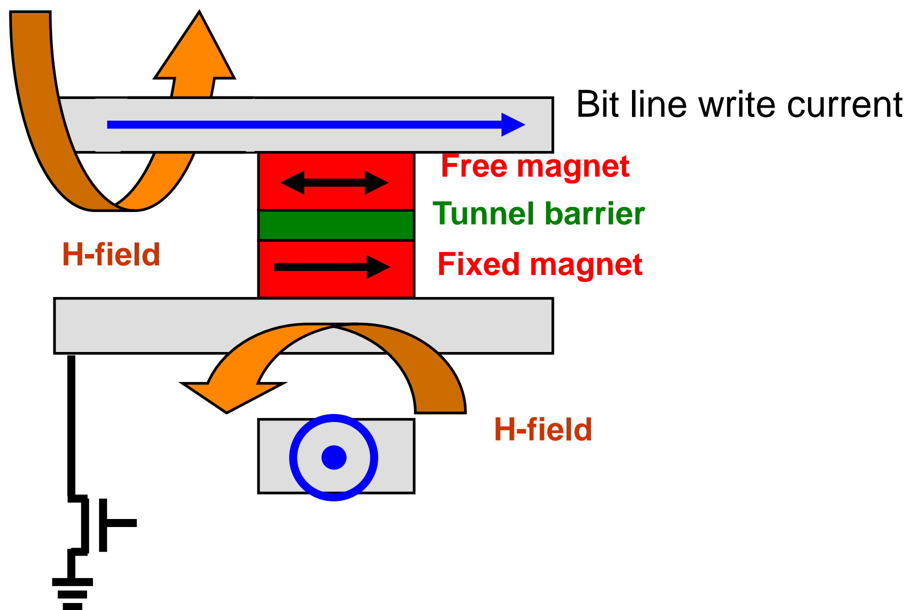
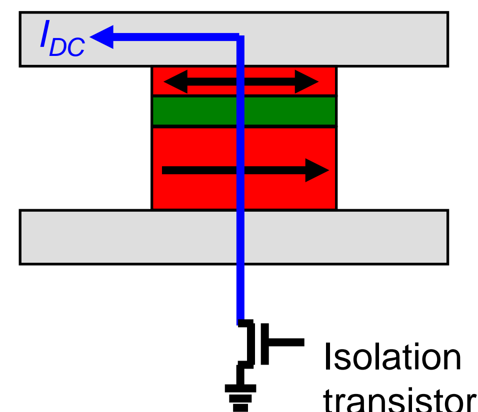
Toggle-MRAM in production



- Cross-point architecture
- Current along bit line and digit line to switch at intersection

ST-MRAM in development



- Current I_{DC} flows through MTJ and transistor
- Fixed magnet polarizes I_{DC}
- Spin-transfer torque programs free magnet
    - Conservation of angular momentum

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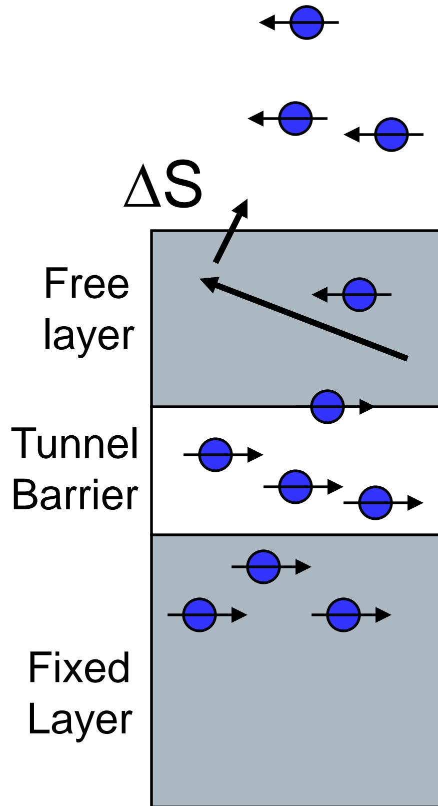
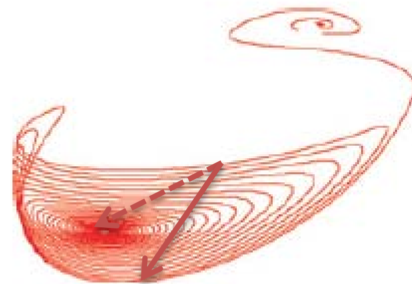
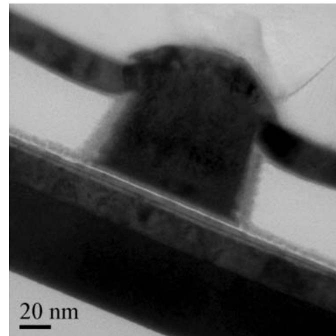
Spin Torque MRAM

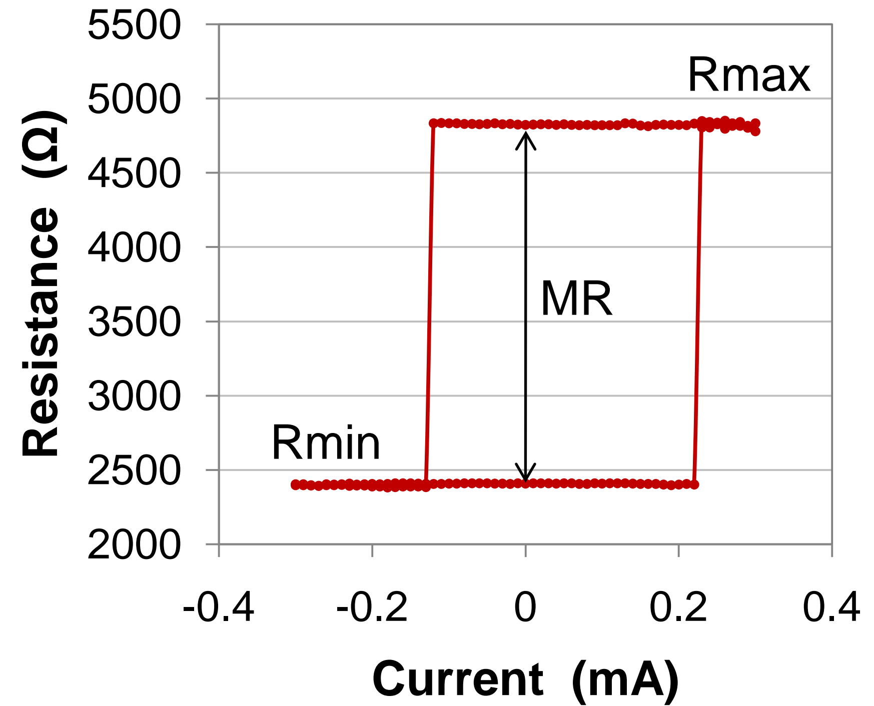
Use spin momentum from current to change direction of *S*, *m*.



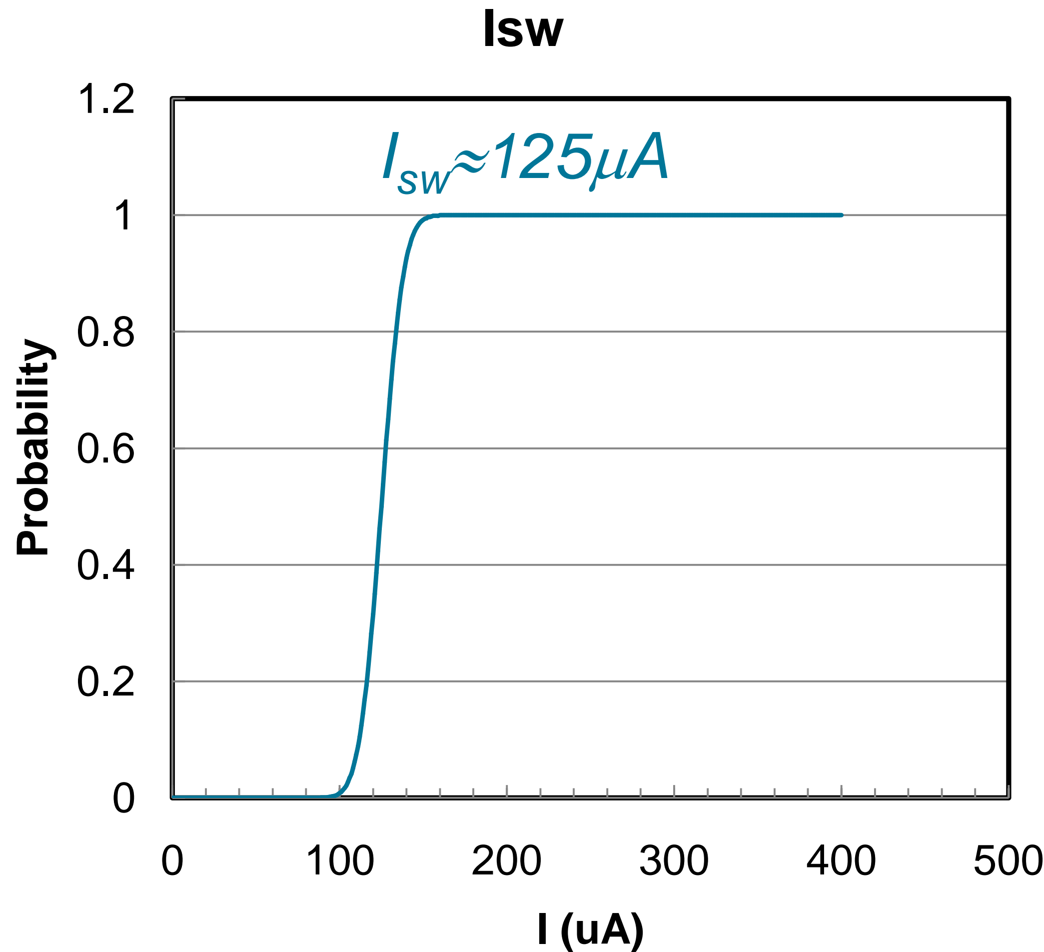
$$\frac{\Delta S}{\Delta t} = Torque$$







Low Switching Current



- **Demonstration of low write current with 60nm bits**
- **Energy barrier = 60kT**

Measured on 16kb CMOS array at t_p = 100ns

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Large Separation of V_{sw} and V_{bd}

16kbit integrated CMOS arrays

Switching Probability

1
0.8
0.6
0.4
0.2
0

Bits switching

Breakdown

Separation ≈ 20σ

100nm x 240nm,
t_p = 100ns

0
1000
2000

Voltage (Volts)

- Excellent separation ≈ 20σ, due in part to $\sigma_{sw} \approx \sigma_{bd} \approx 4\%$

Scaling ST-MRAM

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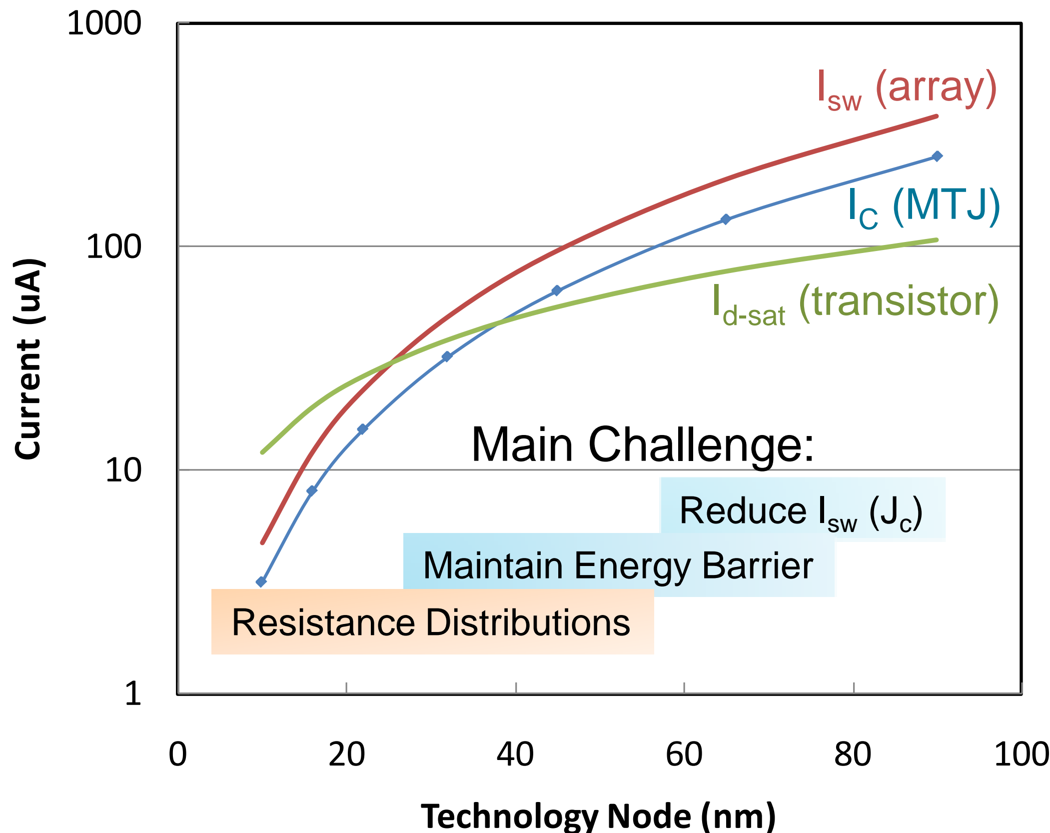
- **Today: Reduce J_c for reliability and smaller transistors**
- **Continued scaling: maintain energy barrier and manage resistance distributions**



- ST-MRAM bits scale favorably to available current from transistor
  - Low Jc for reliability is the bigger issue
- Continued scaling requires innovative magnetic devices and materials
  - Enhanced energy barrier
  - Increased TMR

I_c calculated for J_c=2MA/cm^2

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Memory comparison

	Toggle MRAM (180 nm)	Toggle MRAM (65 nm)*	ST MRAM (65 nm)*	FLASH (65 nm)+	DRAM (65 nm)+	SRAM (65 nm)+
cell size (μm^2)	1.25	0.16	0.04†	0.04	0.03	0.3
Read time (ns)	35	10	10	10 - 50	10	1
Program time	5 ns	5 ns	10 ns	0.1-100 ms	10 ns	1 ns
Program energy/bit	150 pJ	100 pJ	1 pJ	10 nJ	5 pJ Needs refresh	5 pJ
Endurance	$> 10^{15}$	$> 10^{15}$	$>10^{15}$	$> 10^{15}$ read, $> 10^{5}$ write	$> 10^{15}$	$> 10^{15}$
Non-volatility	YES	YES	YES	YES	NO	NO

* 65nm MRAM values are projected
\+ These values are from the ITRS roadmap
† This cell size only considers bit area and ignores CMOS limitations

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Summary

- MRAM is a highly reliable, high-performance, nonvolatile memory ICs, with unlimited endurance
- MRAM has the unique characteristics of a working memory while providing non-volatility
- Current MRAM product densities ranges from 256kb-16Mb
- Continuous advancement in the technology would allow MRAM to drive to higher densities while maintaining its unique characteristics