

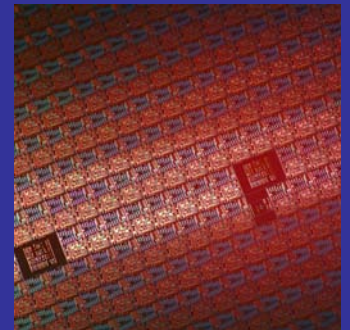


Nonvolatile Memory Seminar
Hot Chips Conference
Memorial Auditorium
Stanford University

Accelerating the next technology revolution

Memory Overview and RRAM Materials Development at SEMATECH

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Director Front End Processes
August 22, 2010



Outline

- NVM Memory Trends & Challenges
- Technology Space for RRAM
- Challenges and SEMATECH RRAM Results

Future trends: Memory for mobile and SOC applications

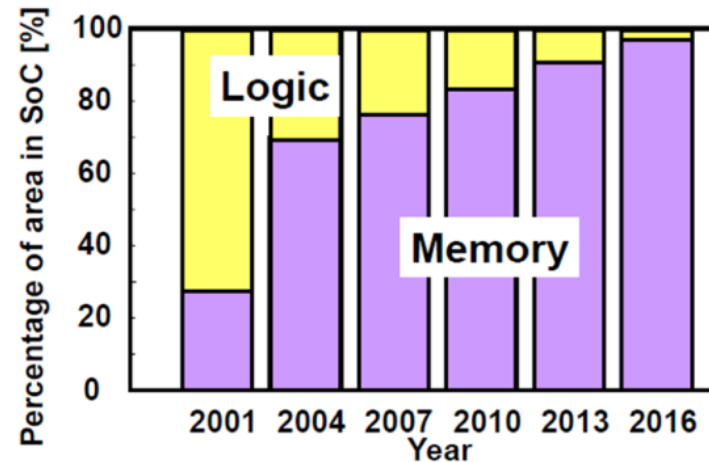


Mobile



High density, low cost, NVM (NAND)

System on Chip (SOC)



Dense, local memory – improve system performance

- IMPACT: High density, low cost NVM important for mobile application
- IMPACT: Local (embedded) memory important for System on Chip

Sub 20nm memory cell, architecture candidates



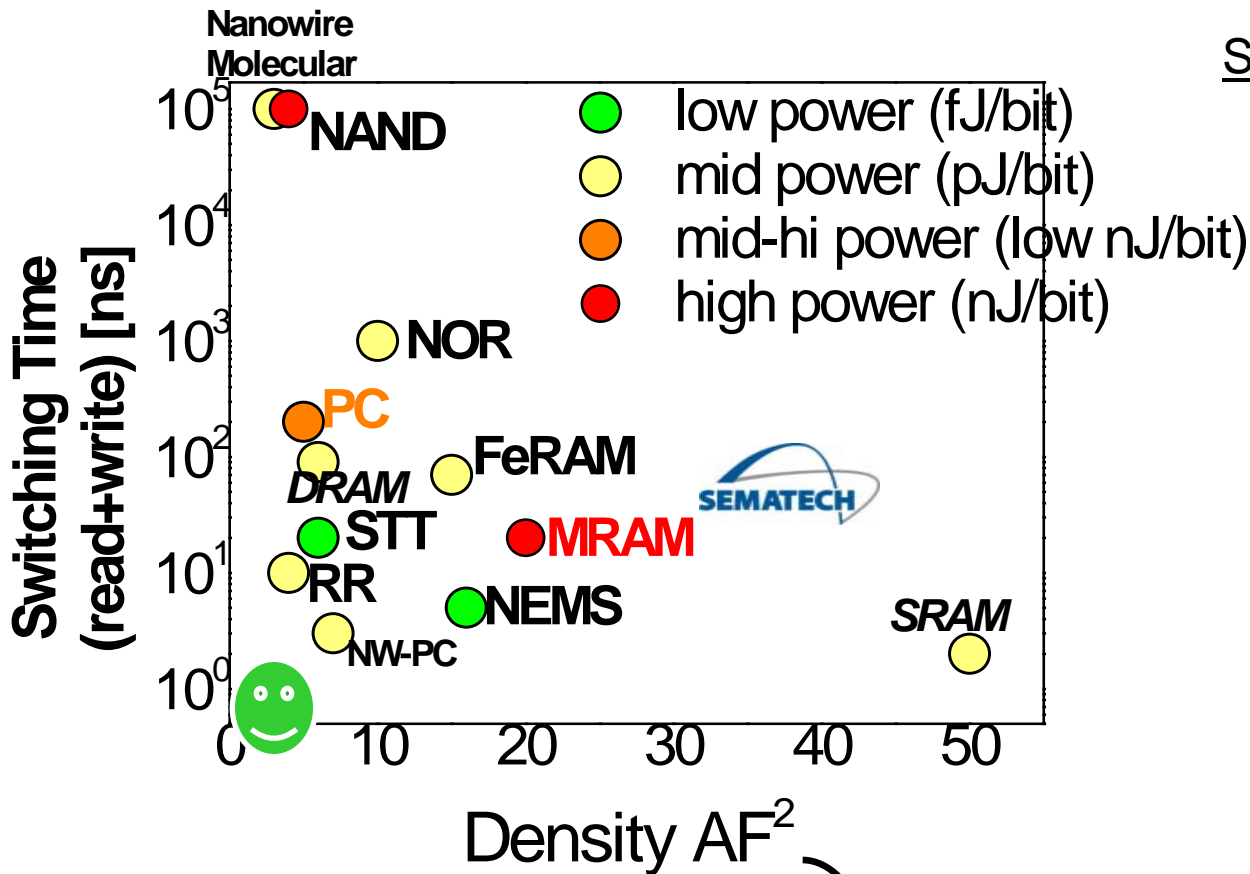
	Advantage	Challenges	“Speculative” Priority	
Cell	Phase Change RAM	• Speed & cost vs. NOR	• Density, Power (Ireset)	production
	SiN / Nano Crystal Charge Trap	• Relatively mature	• difficult to beat floating gate • candidate for 3-D	1
	RRAM	• High speed & density	• Materials, I reset, Reliability	2
	STT-RAM	• endurance, speed , power	• Magnetic domain size effect • Etch difficulty • Challenging materials	2
	Mechanical memory	• Power • Leakage	• Reliable operation • Scalability	4
	Molecular memory	• Density (Molecule size ~nm)	• Poor thermal stability	5
Architecture	Vertical String	• 2-5x lower \$\$ vs. stacked	• deposited tunnel ox • transistor in trench sidewall	1
	Cross bar array	• effective density below $4F^2$	• Litho \$: more costly vs. NAND • selector device	2
	Stacked	• similar to current NAND	• Litho \$: more costly vs. NAND	3

Sub 20nm memory benchmarking

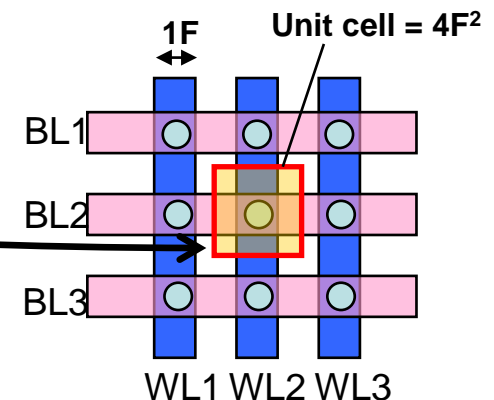


Success Criteria: Future NVM

- MLC = NAND
- Cost structure = NAND
- Function, reliability = NAND
- Density > NAND
- Speed > NAND
- RRAM, STT interesting.



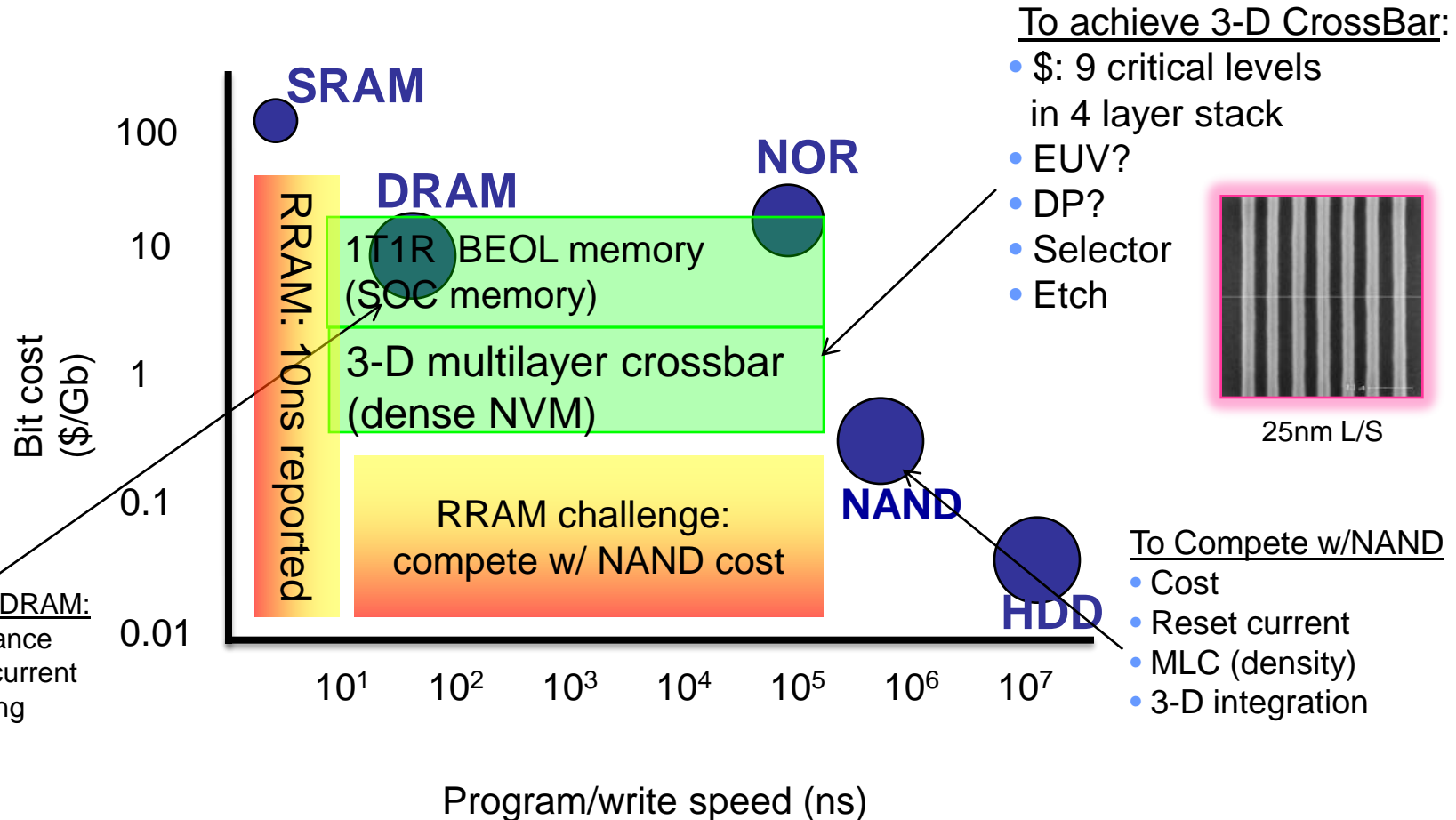
small A = small cell



- [1] W. Y. Choi, and T.-J. King Liu IEDM p. 603 (2007).
- [2] A. Driskill-Smith, Y. Huai Future Fab p. 28 (2007).
- [3] J. E. Green Nature v. 445 p. 414 (2007).
- [4] B. Yu IEEE Trans on Nanotech 7, p. 496 (2008).
- [5] Kryder, et. al. IEEE TRANS ON MAGNETICS, 45, NO. 10, (2009)

Which space should RRAM target?

Associated challenges to compete with DRAM/NAND/NOR



Challenges with RRAM

- Too many materials (manufacturability?)
- Reducing reset currents (power)
- Uniformity
- Endurance
- Integration with selector device (1T1R, 1D1R)

Many RRAM materials: Many not manufacturable



X = Materials in RRAM literature report

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg							

Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

- Many materials risky to put into a semiconductor development line

Which RRAM materials are manufacturing worthy?



X = Materials in RRAM literature report
X = Materials in fabs today

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg							

Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

- Focus on engineering materials that are already in the semiconductor fab (green)

STT-MRAM Materials also challenging

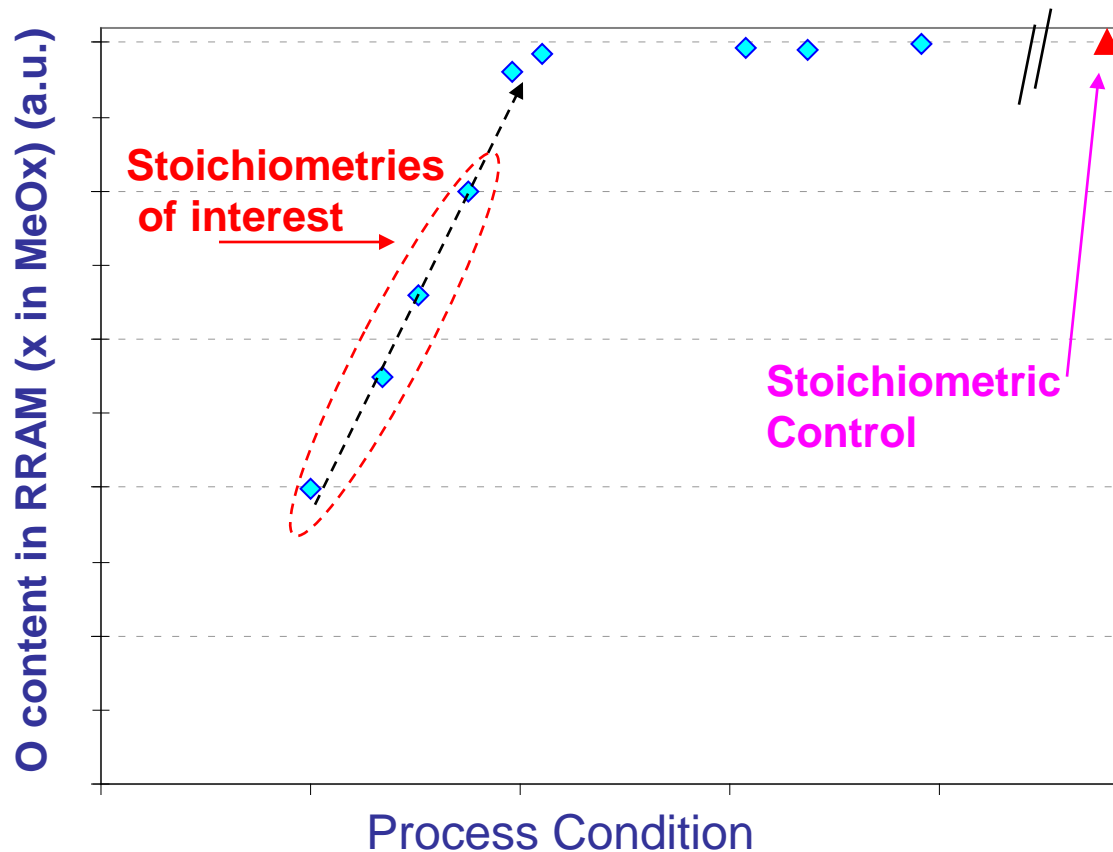


X = Materials in STT-MRAM

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg							

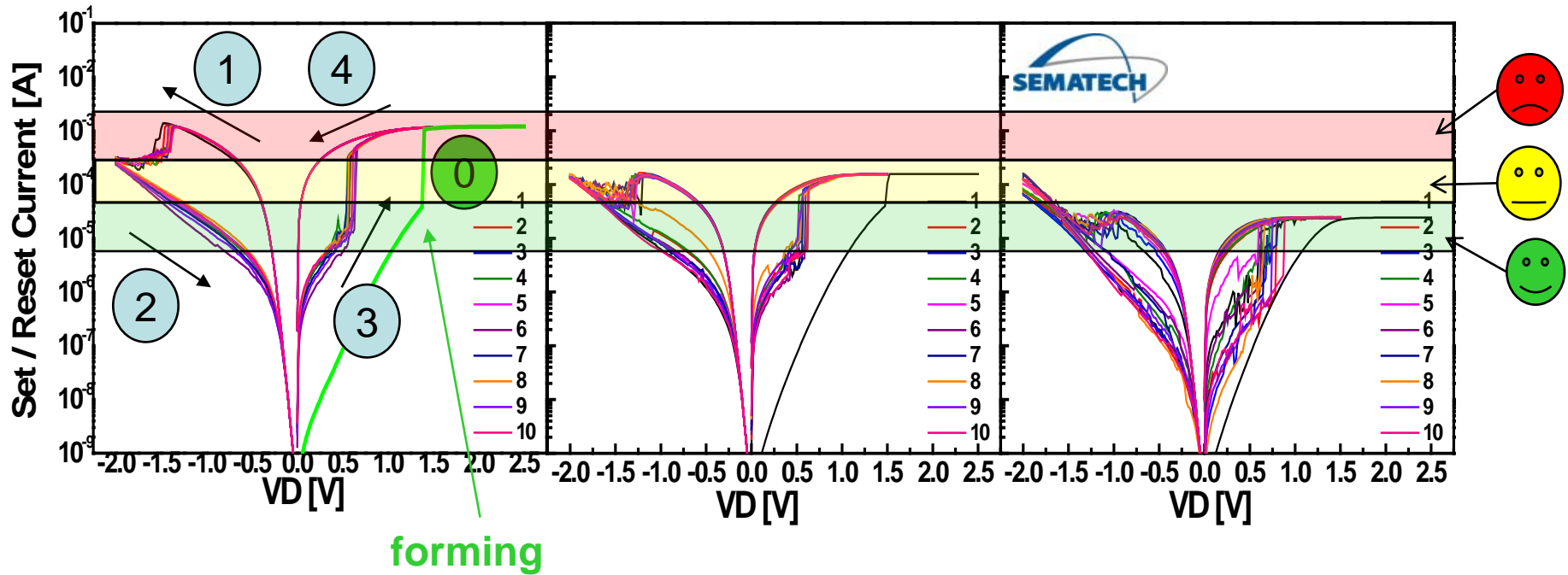
Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

PVD metal oxide RRAM development



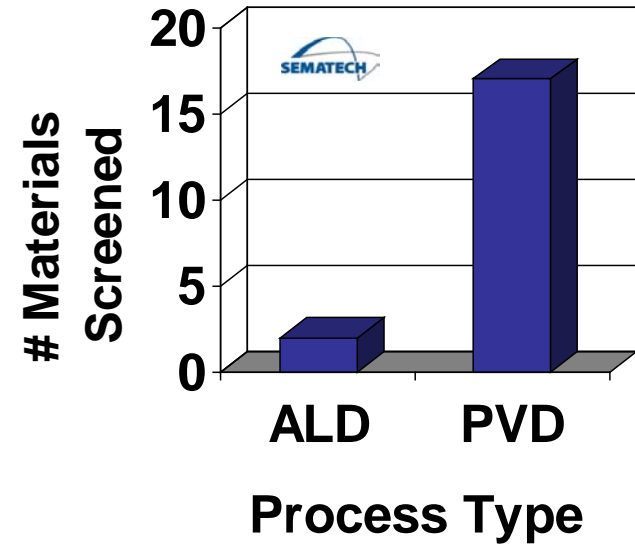
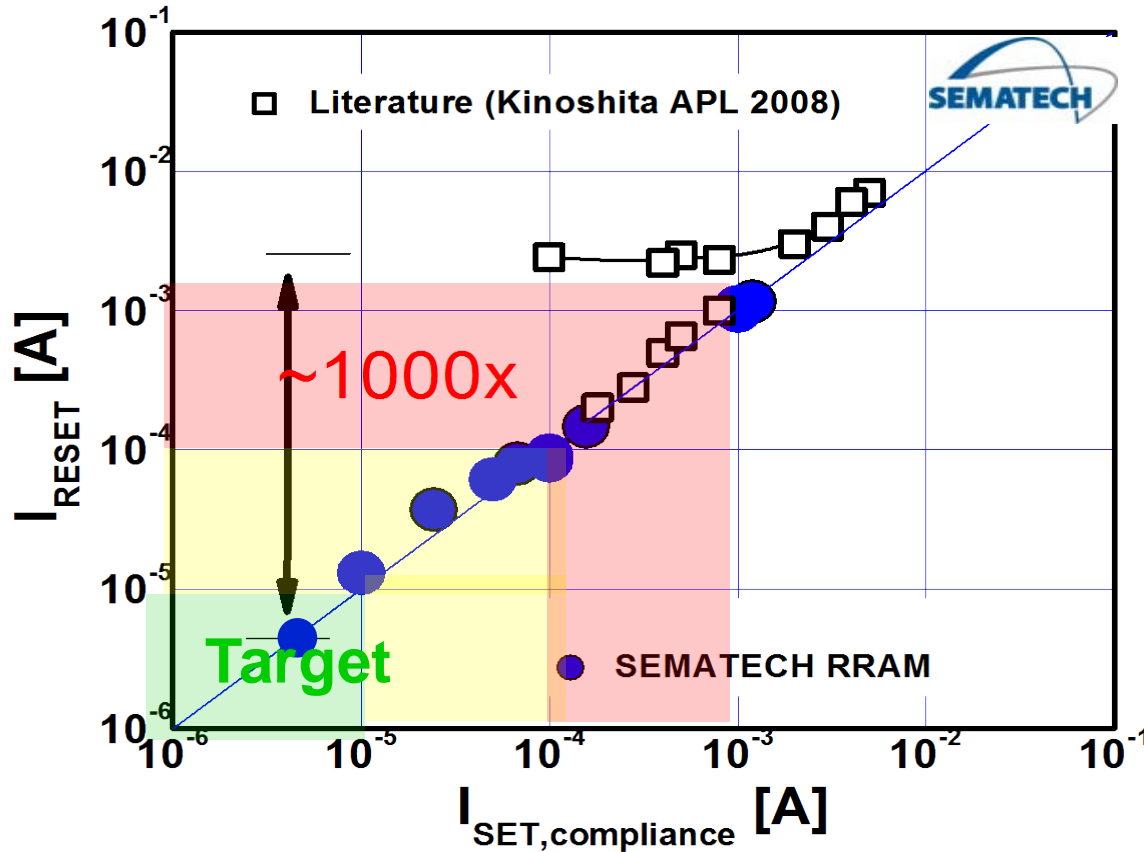
- PVD ideal for Stoichiometry Control, thin, uniform films
- ALD films also developed, but may still need PVD for electrode.
- IMPACT: Correct material Me:O enables correct function.

Progress in reducing reset currents



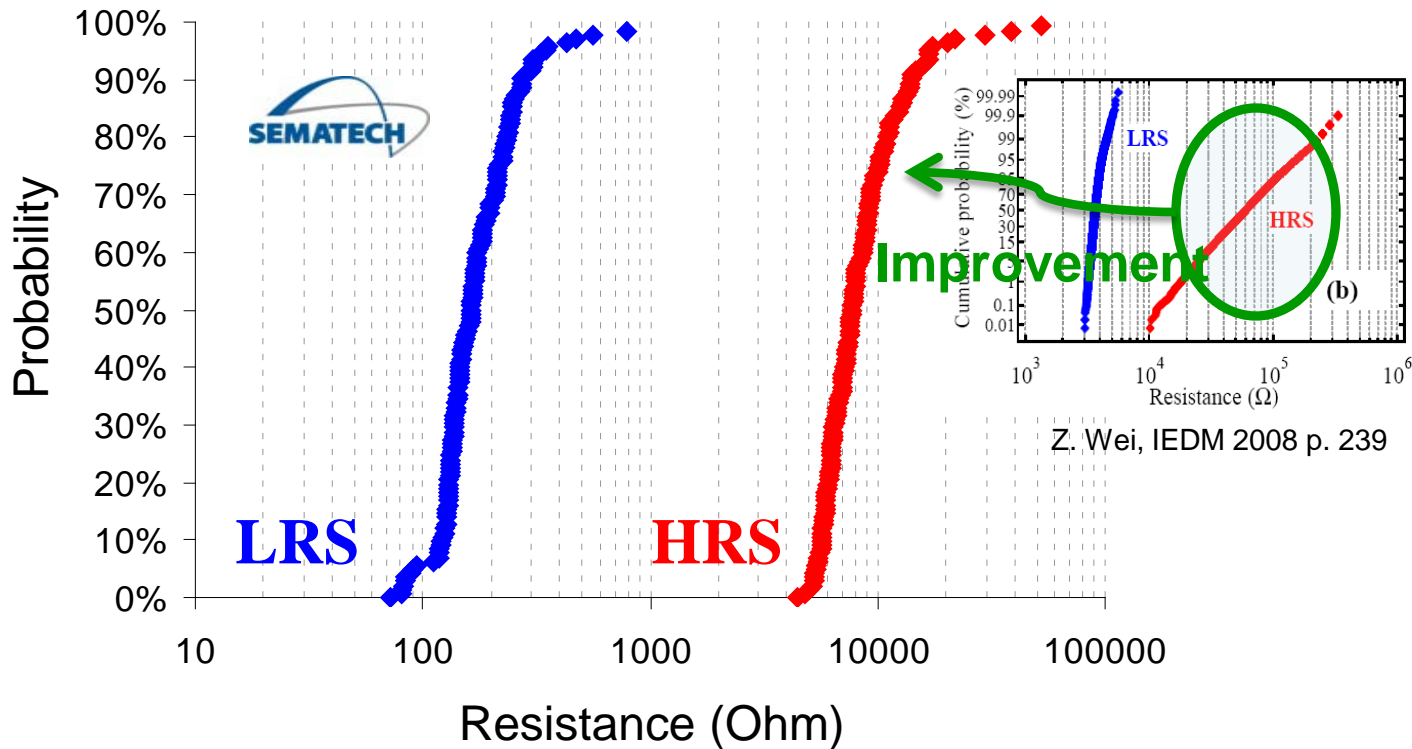
- Resistance switching currents (I_{reset}) improved $\sim 1000\times$.
- I_{reset} improved to $1\sim 10\ \mu\text{A}$ range – desire $10\times$ more improvement.
- IMPACT: Sub $1\ \mu\text{A}$ device likely meets U.S. DARPA target for Switching Energy (fJ/bit)

Reducing Metal oxide RRAM Reset Currents



- SEMATECH has exceeded member company target for 2010 I_{reset}
- 5 micro-amp reset currents achieved with manufacturable metal oxide

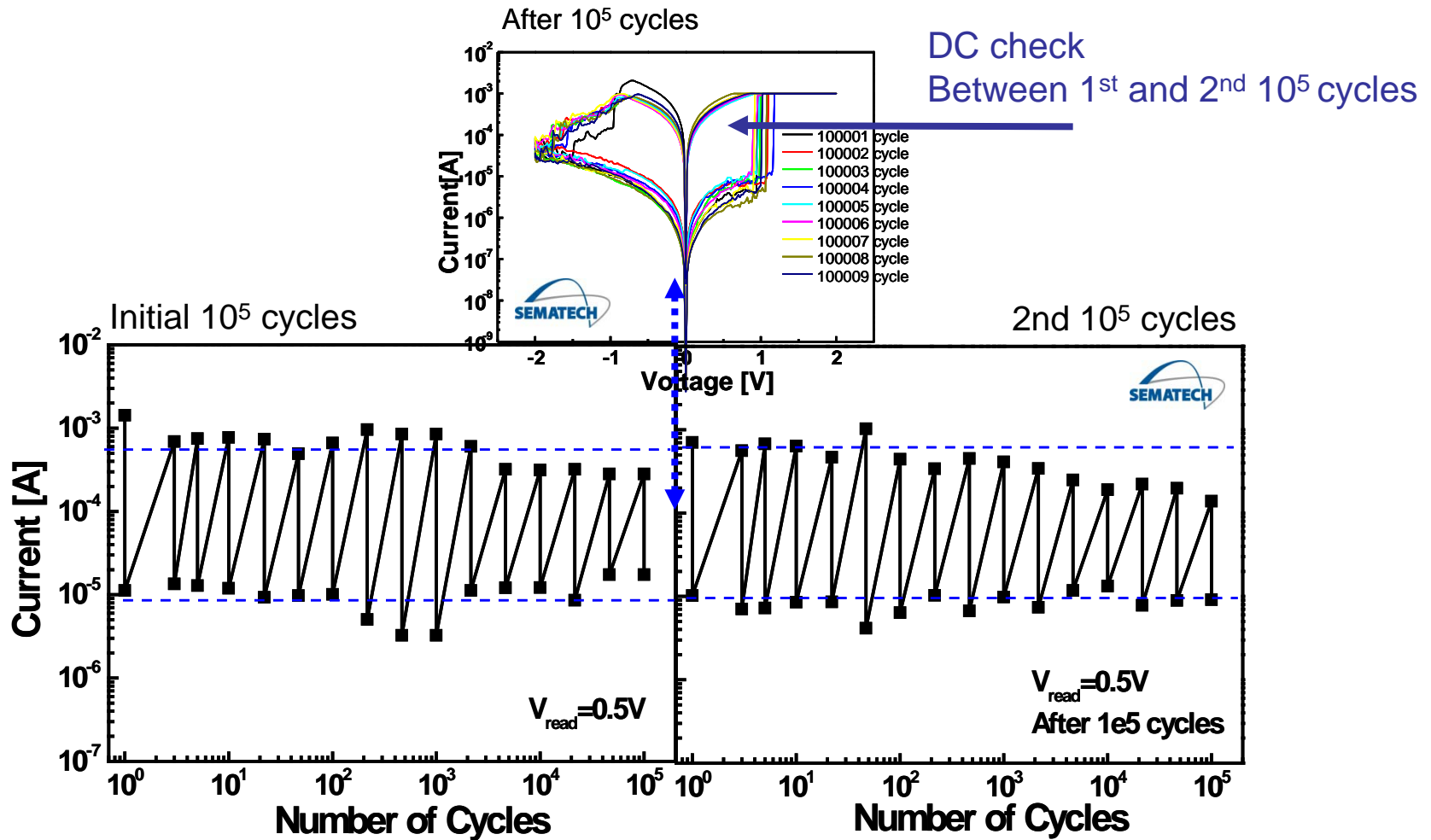
RRAM Reset Uniformity Improves



Z. Wei, IEDM 2008 p. 239

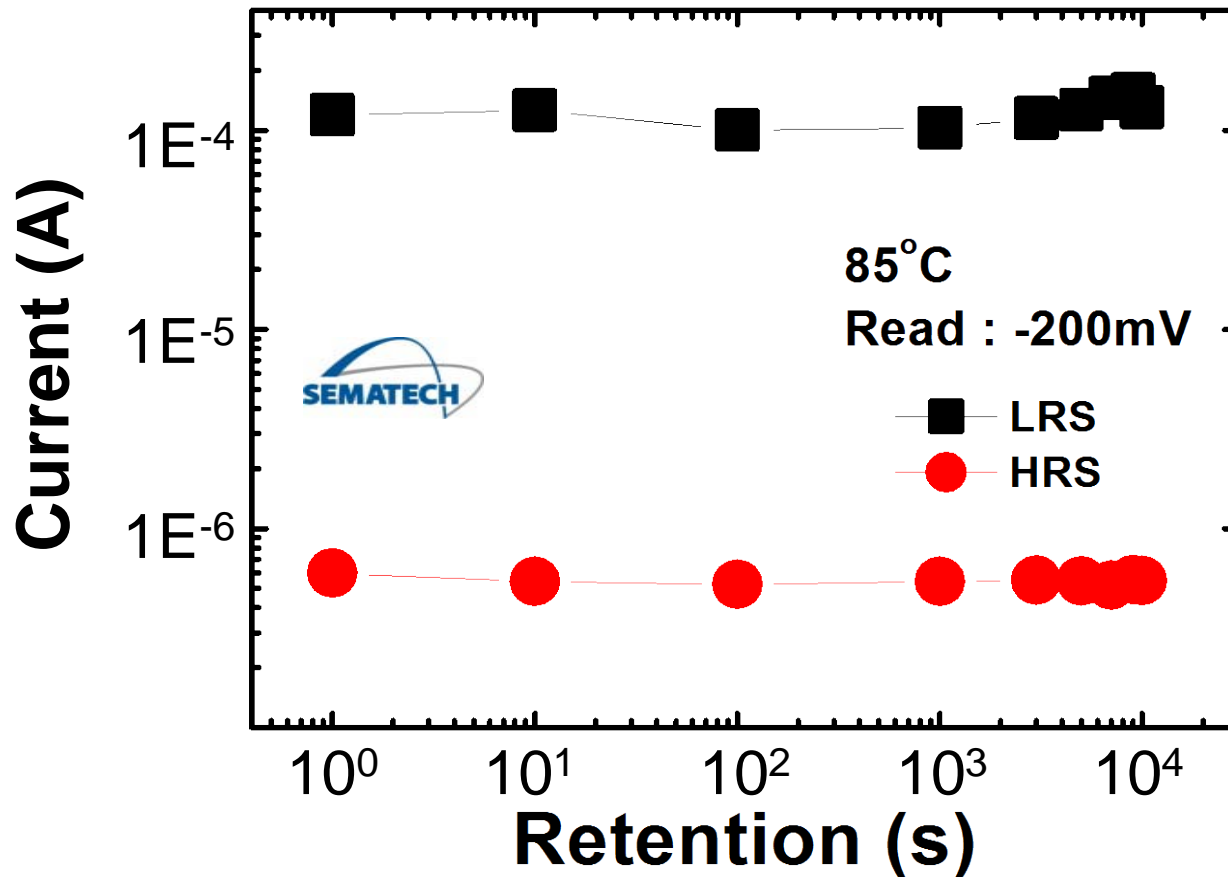
- Uniformity of High Resistance state improve across wafer (>300pts).
- IMPACT: Uniformity is key issue for Manufacturability - Multilevel Cell

Encouraging RRAM endurance check



- Good initial RRAM cycling (2×10^5 +) – much work to do yet
- **IMPACT:** If RRAM achieves fJ/bit and 10^{15} cycles it competes with DRAM

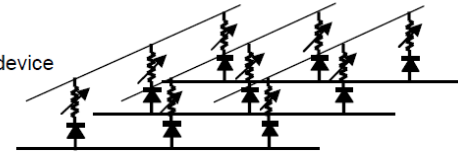
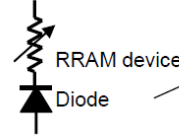
Metal oxide RRAM has demonstrated reasonable retention



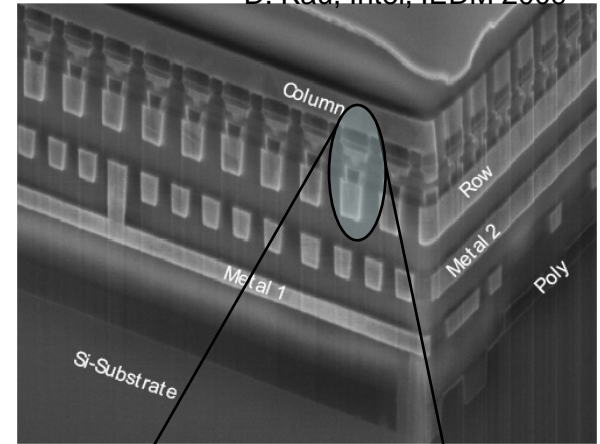
- Further work needed on devices meeting I_{reset} , but encouraging initial data.

Selector Challenge

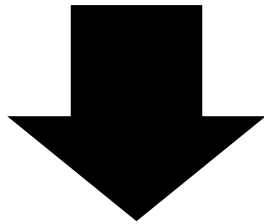
1D1R



D. Kau, Intel, IEDM 2009



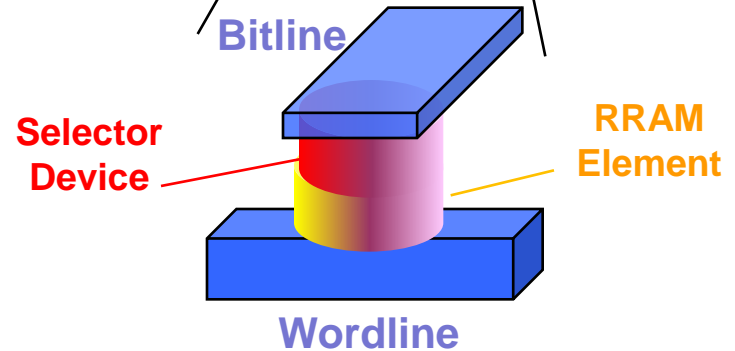
Trade-off



Reduce
RRAM Reset
Currents
 $<1\mu\text{A}$



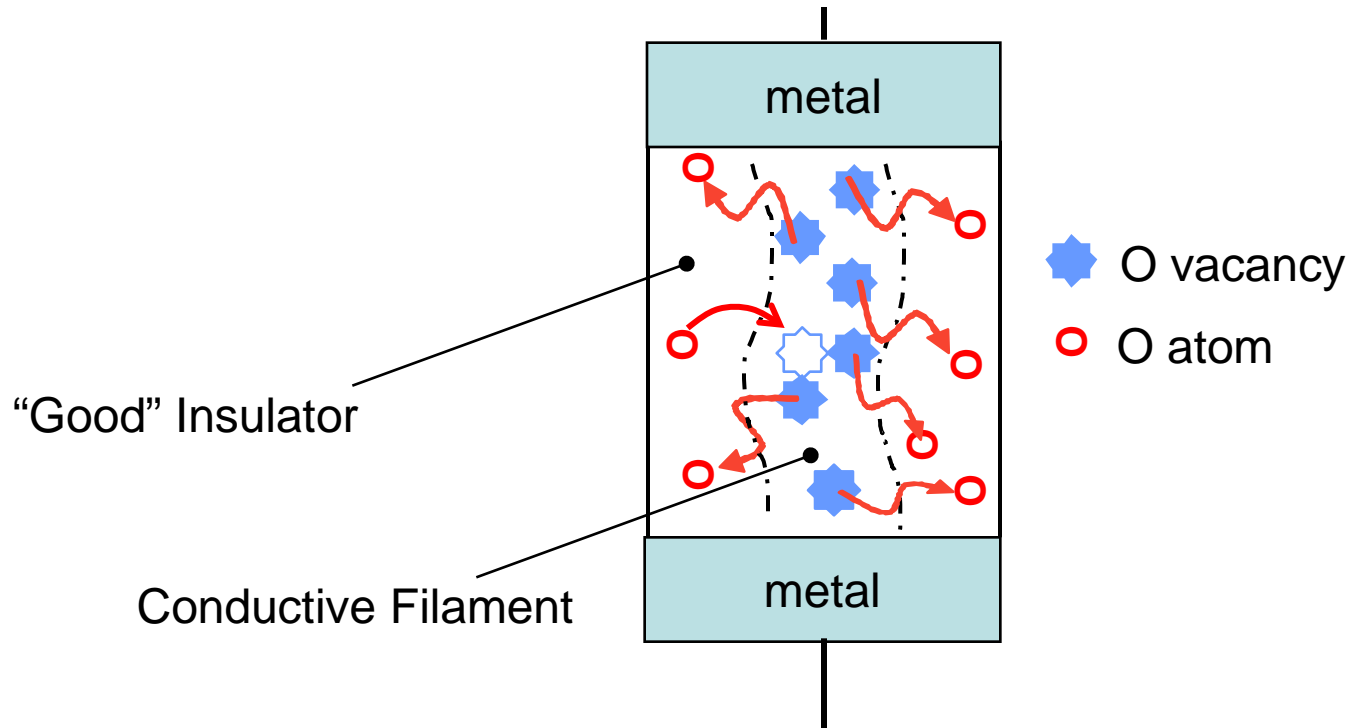
Relax
Selector
Drive Needs
 $<10^6 \text{ A/cm}^2$



- Why does reset current matter?
 - SELECTOR \rightarrow lesser I_{reset} means lesser diode current requirements
 - IMPACT: Selector flexibility eases challenge of array integration

Basic metal oxide RRAM Mechanism

Binary oxides: filament formation



- **Switching, retention, endurance controlled by defects**
- **IMPACT: Need to understand details for reliable product**

SEMATECH test structure

Test structure allows reproducible electrical / reliability data

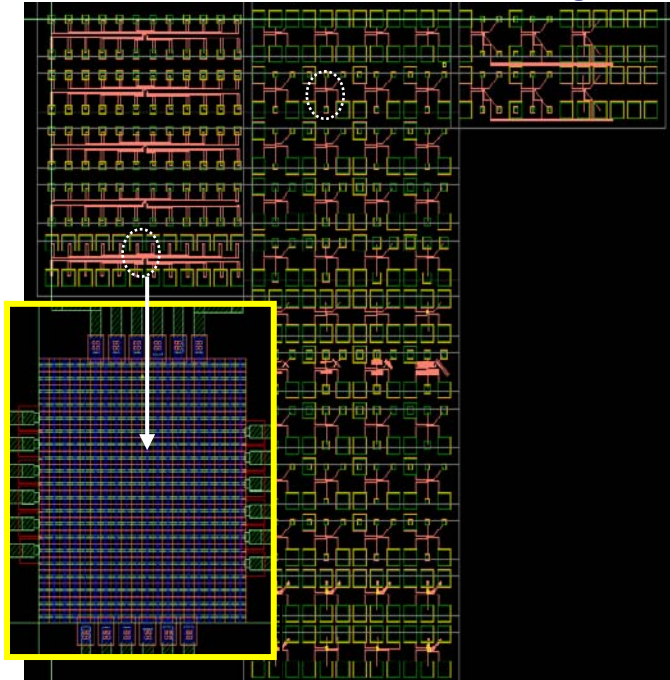


Test Structure	Structure	Purpose
1. Contact-type MIM structure (x-section)		<ul style="list-style-type: none"> • Quick materials studies
2. Stack-type MIM structure (X-section)		<ul style="list-style-type: none"> • Quick materials studies
3. 1T1R test structure (top view)		<ul style="list-style-type: none"> • Iso 1T1R, Iso 1R, • Cross Pt Array 1T1R • Detailed I_{reset} studies • Detailed parasitic studies • Array retention, endurance • 25nm x 25nm CD

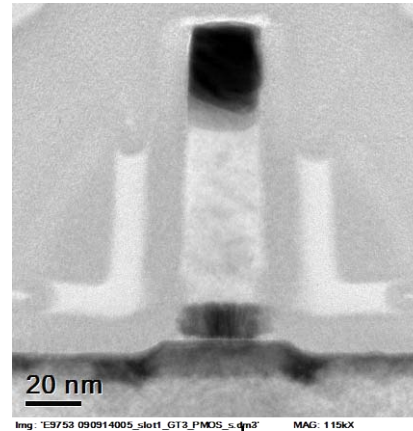
Overview of SEMATECH capabilities



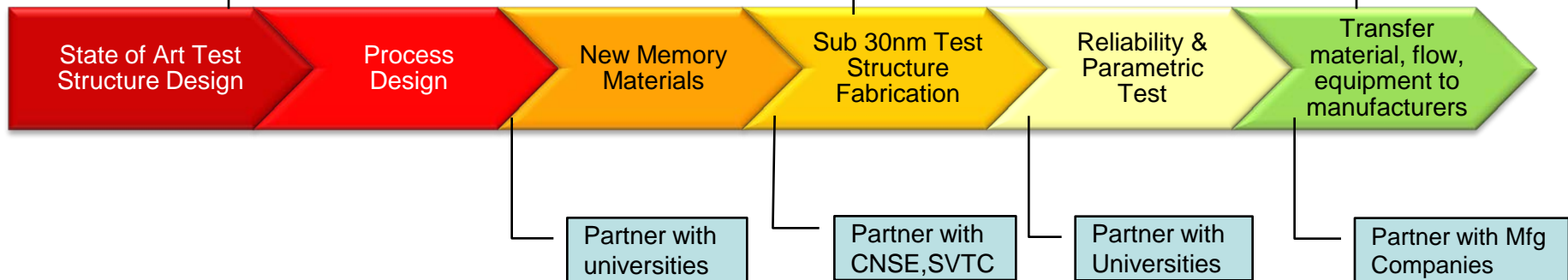
SEMATECH 1T1R Test Pattern Design



SEMATECH 20nm Nano Devices



SEMATECH Mfg Members Use Modules



Conclusions



- Planar floating gate will be pushed to 2X nm.
- RRAM may compete as SOC memory (BEOL).
- RRAM may fit between NAND & DRAM cost space (stand alone)
 - Cost will be key
 - $4F^2$ cell with ~4 levels achieve effective $1F^2$ (MLC necessary)
- Materials challenges addressed
 - Manufacturable MeOx and electrode
 - Reset / set currents are approaching acceptable levels (1 micro-amp)
 - Improved Uniformity Encouraging
 - Endurance, retention are promising, need improvement $>1e5$ cycles
 - Selector device and polar / bipolar design are challenges
- Quality test structures (1T1R) assist in accurate characterization, development