

# The new Xbox 360 250GB CPU GPU SoC

Rune Jensen, Microsoft  
Bob Drehmel, IBM

Hot Chips 22  
8/23/2010



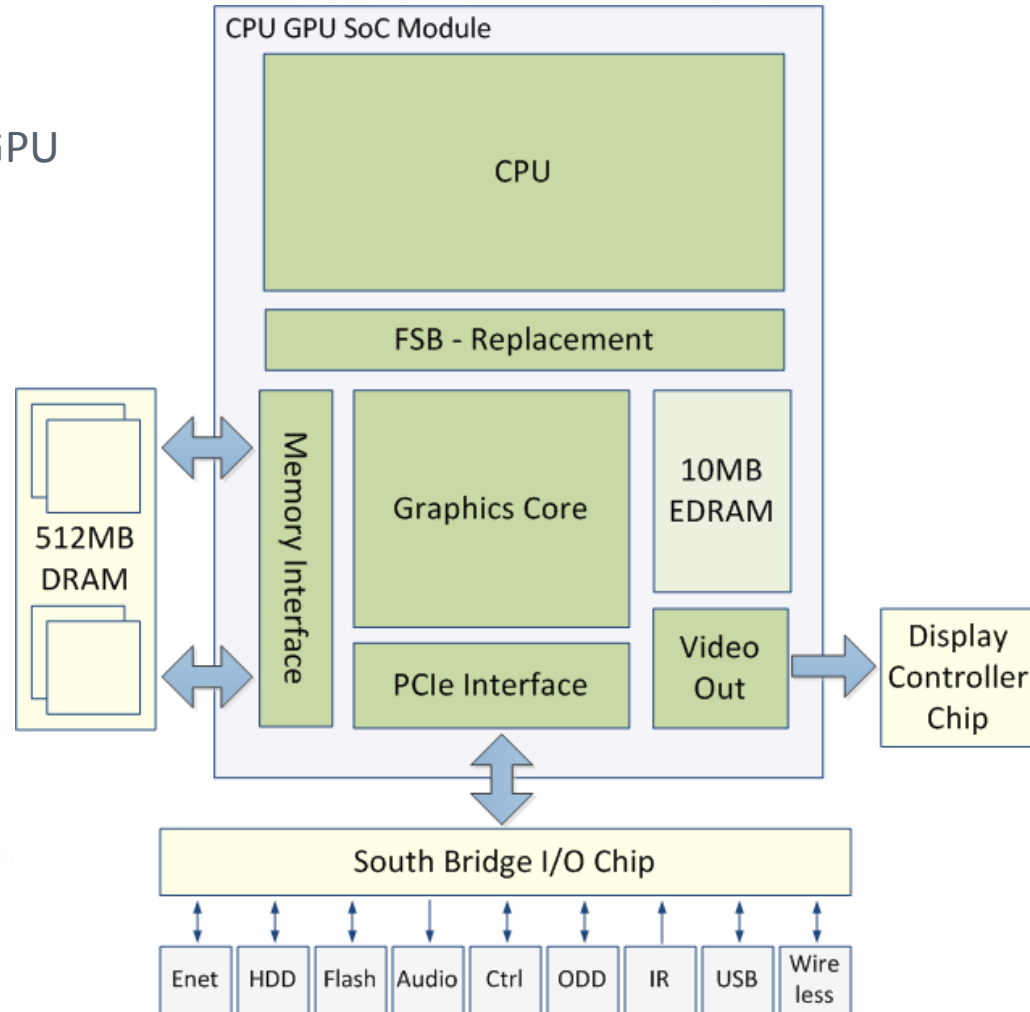
**Microsoft**<sup>®</sup>

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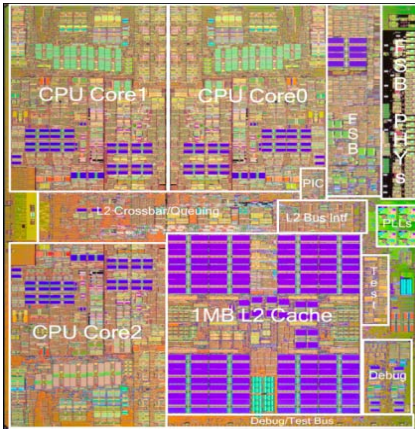
# Xbox 360 250GB System

- CPU GPU SoC Module
  - CPU GPU Die
    - High Performance CPU & GPU
    - GDDR3 Memory Interface
    - Video Output
    - PCIe
  - Embedded DRAM Die
- Custom South Bridge
  - IO Connectivity
  - System Management
- Custom Video Display Controller
- Optical Disk Drive
- Flash and IO Connectivity
- 250GB HDD
- Wireless 802.11N Integration

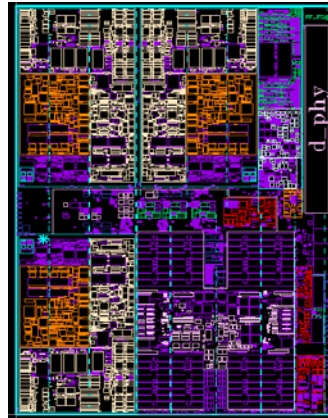


# CPU, GPU Process Migrations

CPU



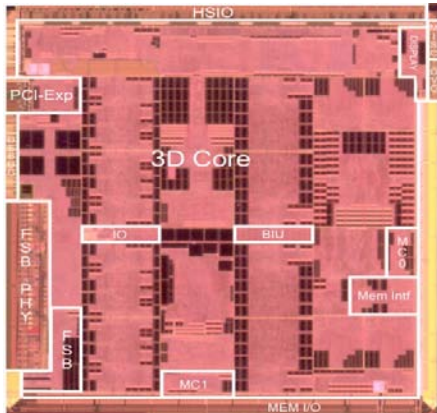
90nm, 2005



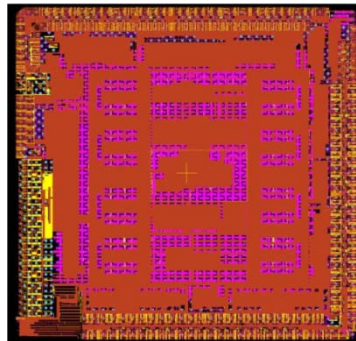
65nm, 2007



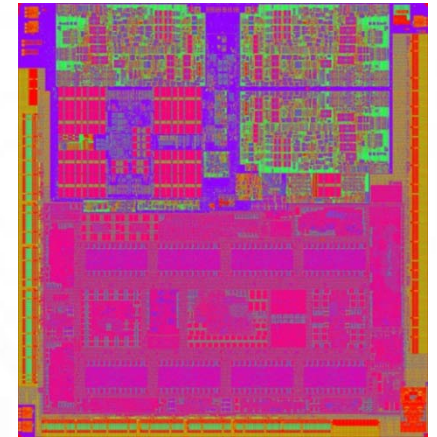
GPU



90nm, 2005



65nm, 2008



45nm, 2010

# Motivation for Integrated CPU GPU SoC

## ○ Cost and Power Savings

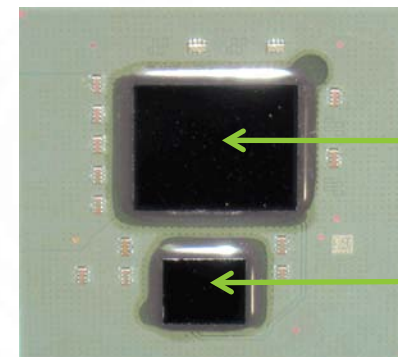
- Front Side Bus Removal
- Single Package
- IBM 45nm SOI Technology

## ○ Simplified Console Design

- Motherboard Footprint
- Power Delivery
- Thermal Design
  - Single Heatsink + Fan



35x35mm Package,  
1156 Balls



Integrated  
CPU GPU

Embedded  
DRAM

# CPU GPU SoC: Features & Block Diagram

## CPU

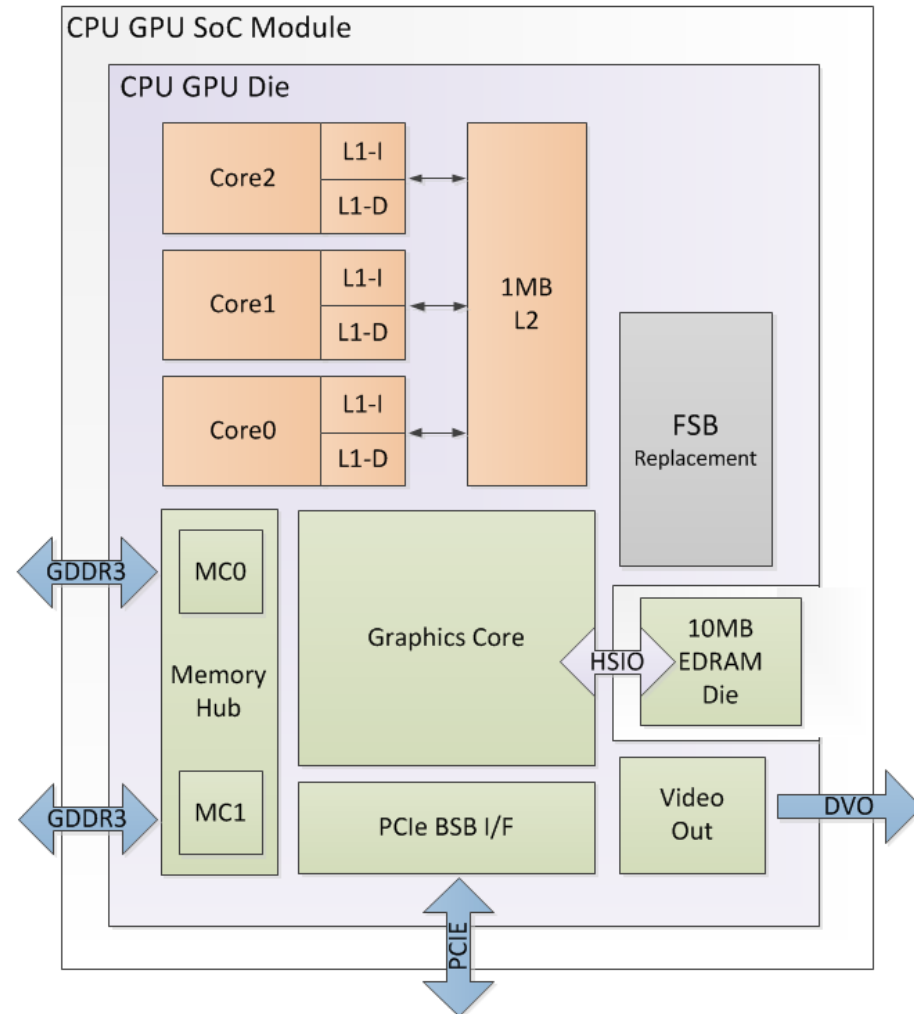
- Three 3.2 GHz PowerPC® cores
- Shared 1MB L2 cache
- Per Core:
  - Dual Thread Execution
  - 32K L1 I-cache, 32K L1 D-cache
  - 2-issue per cycle
  - Branch, Integer, Load/Store Units
  - VMX128 Units enhanced for games

## GPU

- 48 parallel unified shaders
- 24 billion shader instructions per second
- 4 billion pixels/sec pixel fill rate
- 500 million triangles/sec geometry rate
- High Speed IO interface to 10 MB EDRAM

## Compatibility

- Functional and Performance equivalent to prior Xbox 360 GPU/CPU
- FSB Latency and BW match prior FSB



# Technology

## Chip Statistics

- 372M transistors
- 45nm SOI, Ultra-low k dielectric
- 10 levels of metal
- 153 array types, ~1000 instances
- 1.8 million flip flops
- 6 PLLs
- 12 clock domains
- Compared to 2005 CPU GPU
  - >60% Power Reduction
  - >50% Silicon Area Reduction

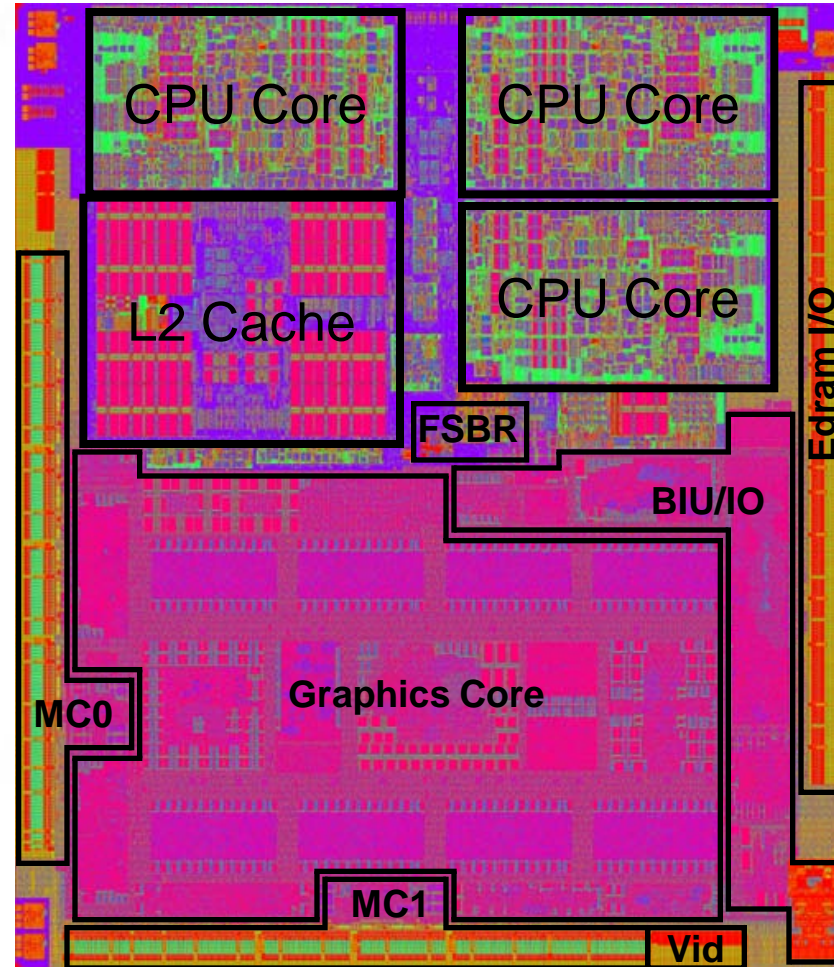
## Package Technology

- 35mm FC-PBGA (3-2-3) build-up layers
- Lidded Multi-Chip Module
- High speed interface to on-module EDRAM
- C4 Pitch: 151um minimum

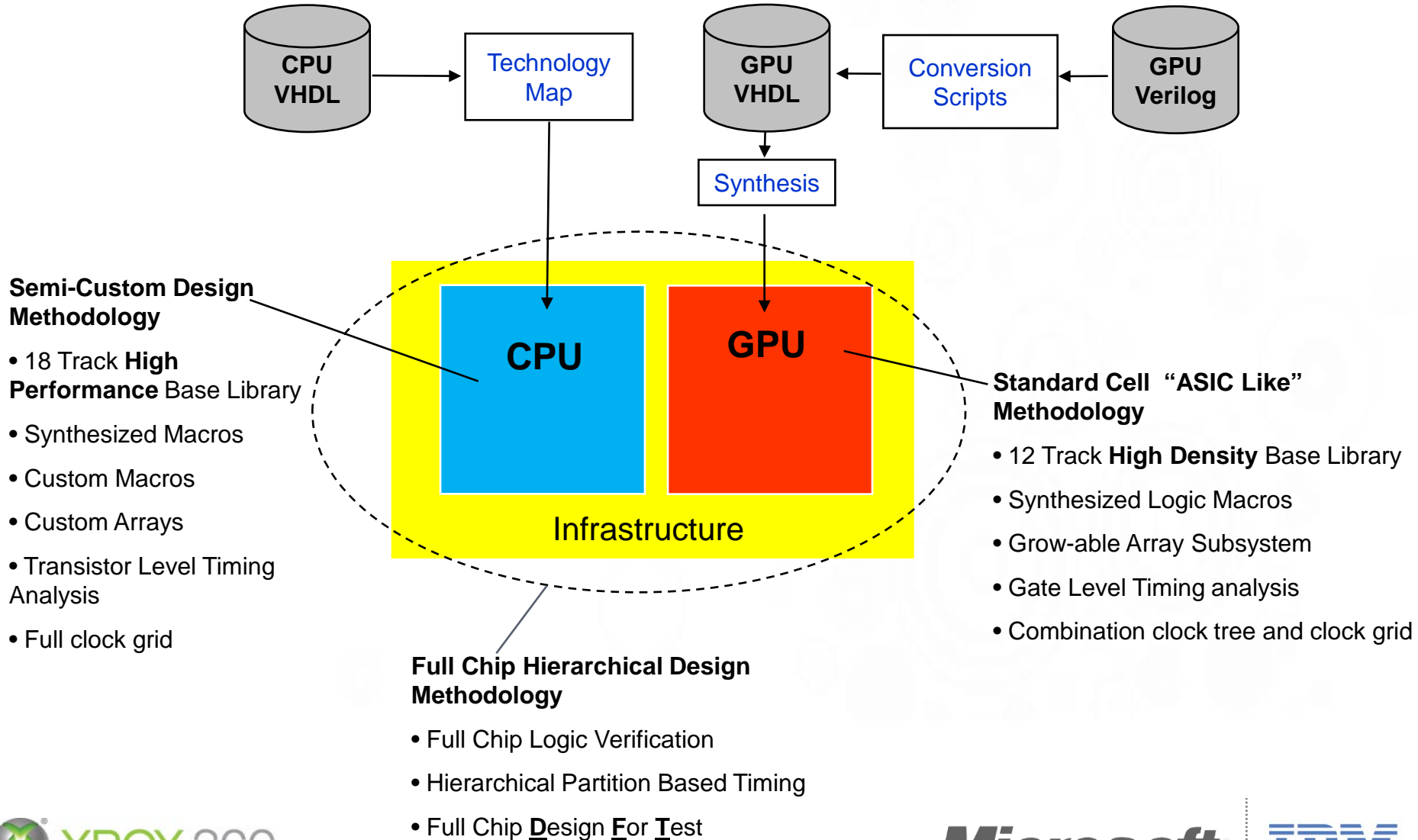
## Power Delivery

- Adaptive Power Supply (APS)
- 8 Power Domains

## Manufactured by multiple foundries

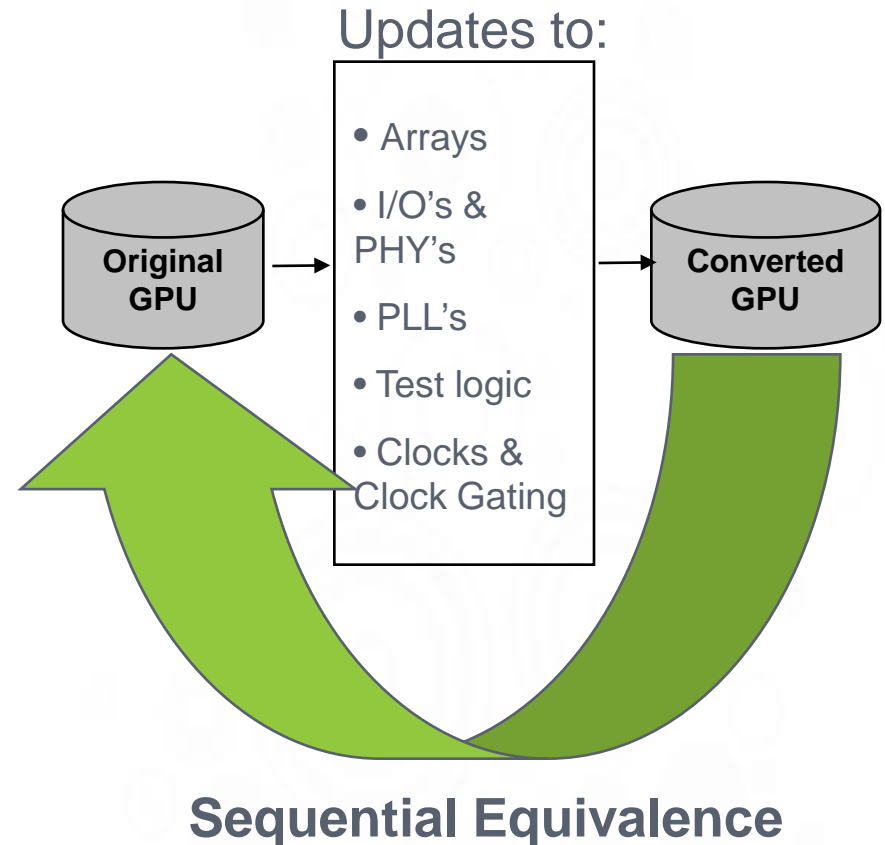


# Implementation Challenge: High Performance + Density



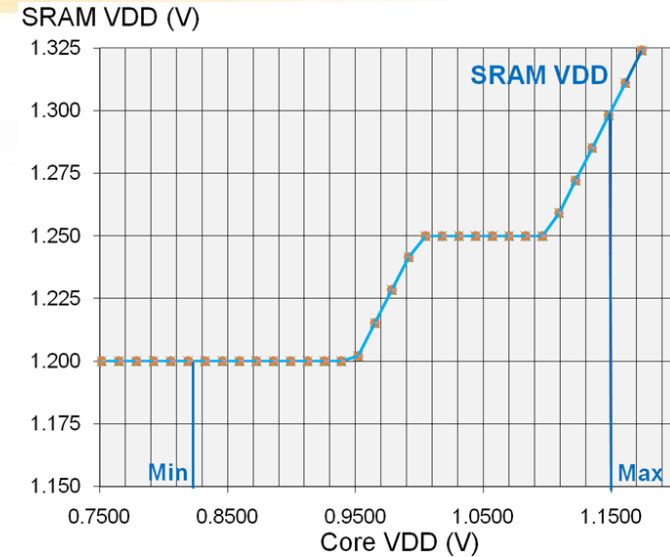
# Implementation Challenge: Backward Compatibility

- **Challenge: The new hardware must be 'transparent' to the user**
  - Backward Compatibility is a combination of both performance and function
  - Existing verification environments only validate function
  - Problem compounded by new chip boundaries and technology change
- **Solution: Sequential equivalence used to validate design migration**
  - Compare corresponding sequential path outputs from two different design representations to ensure their function is the same
  - Provides both performance and functional validation for units that didn't change
  - Leveraged IBM developed tool for functional equivalence
- **Solution: Pattern based verification used to focus on any areas of change**
  - Ran existing pattern based test cases to validate functions
  - Wrote new test cases for any areas of change, including the new FSB logic

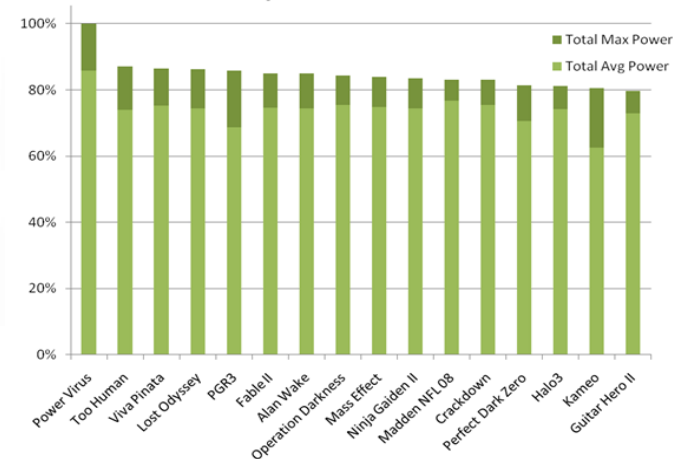


# Power Optimization

- Power Optimization Key Design Requirement
- Adaptive Power Supply
  - Part specific supply voltage for Core VDD
  - Separate SRAM supply tracking Core VDD
  - Power saving of 31%
- In System Voltage Regulator Calibration
  - Regulator loadline and tolerance calibrated
  - Ring Oscillator based on-die voltage measurement
  - Power saving of 12%
- Total Power Saving 43%
- Max Power Application – Power Virus
  - Combine CPU + GPU Max Usage
  - Power virus >10% more aggressive than games

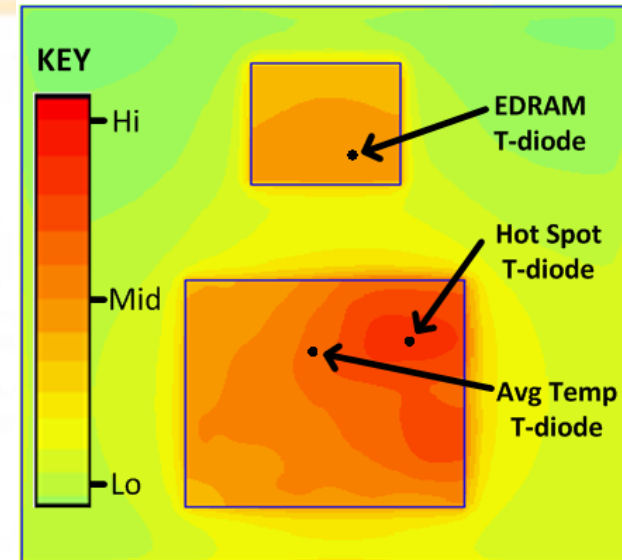


Example Game Power Consumption Compared to Power Virus



# Thermal Management

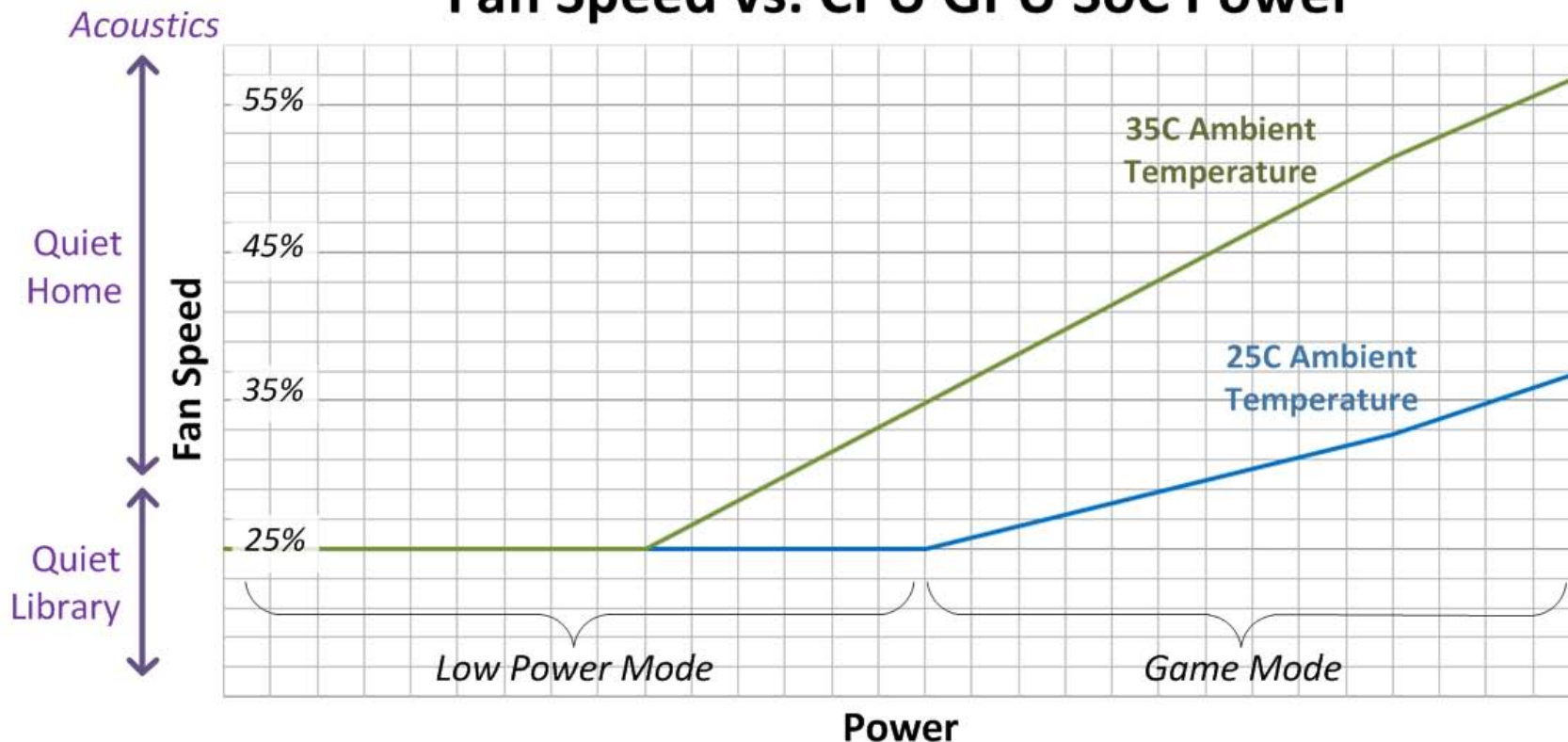
- Requirement: Max hot spot & Max average temperature
  - Must be met regardless of workload
- Power and Thermal Maps created for extreme use cases
  - Combinations of Max/Min CPU and GPU power
- Thermal diode placement dictated by use cases
  - Hot Spot Diode: Between CPU core0 and 1
  - Average Temperature Diode: By GPU shaders
  - Separate Diode for EDRAM
- Thermal set points to ensure ample margin to requirements
  - Closed loop operation based on all T-Diode measurements
  - Goal to keep fan speed low.
  - Set points reduced in low power mode to reduce thermal overshoot when switching to full power mode
- Result: Thermal requirements met



*Example Thermal Map*

# Results from Power and Thermal Optimizations

## Fan Speed vs. CPU GPU SoC Power



# Console Design Using CPU GPU SoC

## ○ Power Reduction

- Smaller Power Supply Unit

## ○ Simplified Motherboard Layout

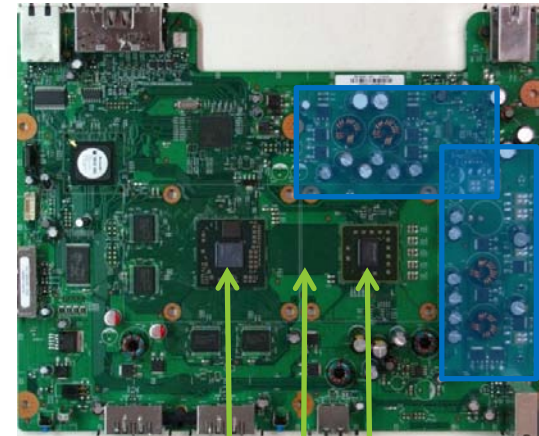
- Single Chip for CPU GPU
- Power Delivery
- Efficient decoupling cap placement

## ○ Thermal Flexibility

- Single Heatsink
- Single Fan

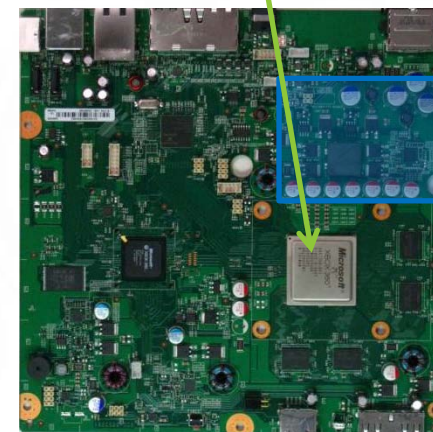
## ○ Console Size Reduction

Existing Xbox 360 Motherboard



GPU FSB CPU

Power Delivery



Motherboard with CPU GPU SoC

# Console Design Using CPU GPU SoC

## ○ Power Reduction

- Smaller Power Supply Unit

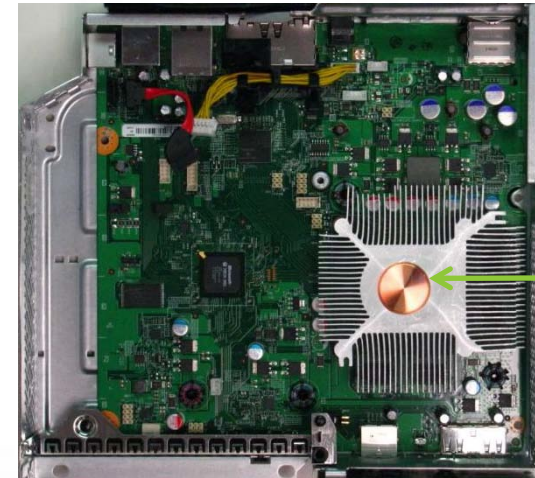
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## ○ Console Size Reduction



Motherboard + Heatsink

# Console Design Using CPU GPU SoC

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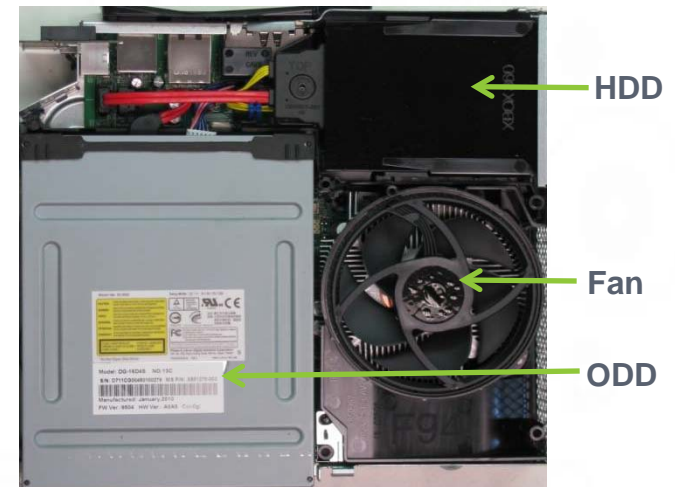
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## ○ Console Size Reduction



Motherboard, Fan, Optical Disk Drive

# Console Design Using CPU GPU SoC

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## ○ Console Size Reduction



New Xbox 360 250GB Console

# Conclusion

- First High Performance Integrated CPU GPU SoC
  - 372M Transistors
  - IBM 45nm SOI Technology
- Enabled Whisper Quiet Console
  - Optimized Power and Thermal Design
- Significant benefits achieved from close collaboration of system and chip design teams



# Appendix

## Contributing Authors

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