



Taking semiconductors
to the next level

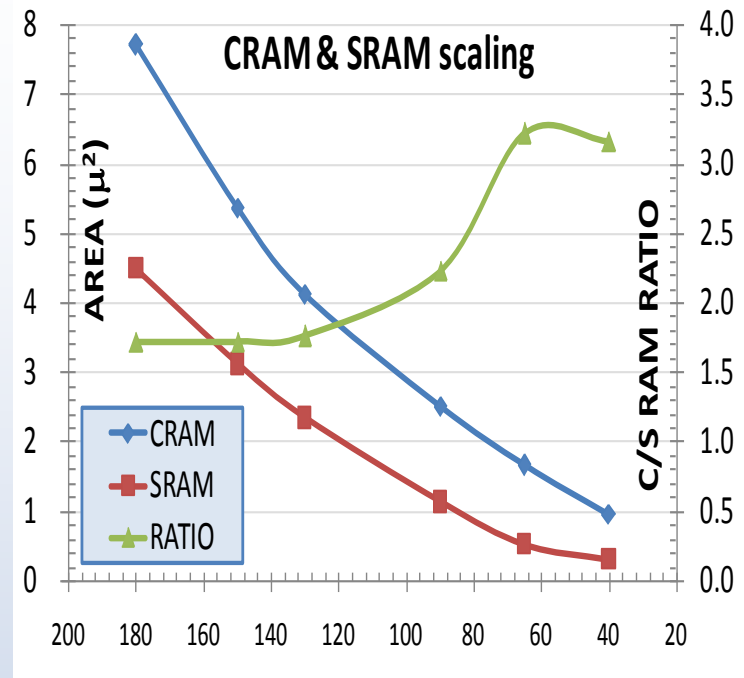
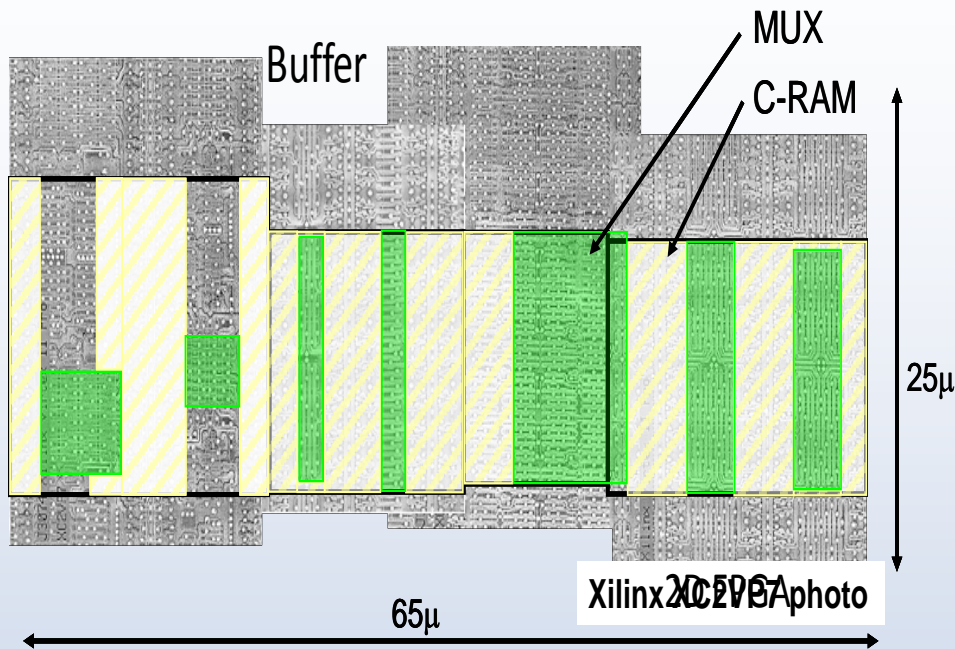
3D FPGA & 3D ASIC

Worlds first unified 3D IC design platform

Raminda Madurawe

Hot Chips, August 2010

2D FPGA dilemma

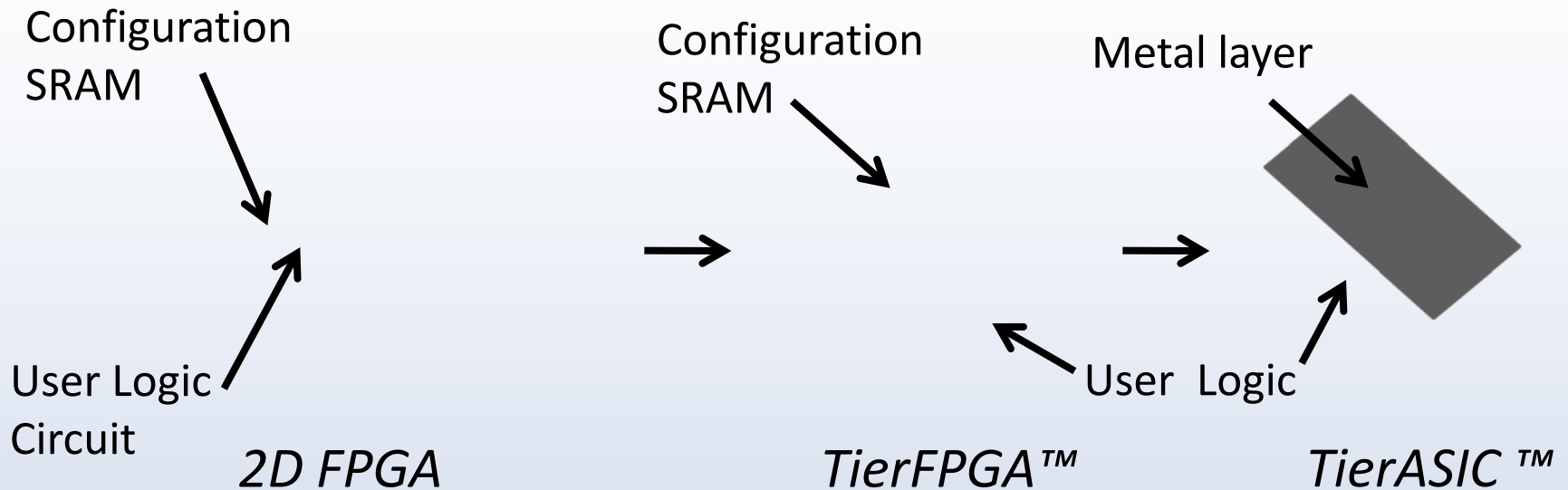


CRAM = configuration SRAM

- Large programming overhead
 - Longer wires = degradation
 - Removing overhead = 2nd design

- 20 years of SRAM scaling
 - CRAM > memory SRAM
 - Stability / disturb at 28nm?

3D Product concepts



- 2D FPGA – poor area, cost, power, speed
- 3D FPGA – better area, power, cost, speed
 - Same placement / wires / base die 3D ASIC™
 - One design – one timing closure – FPGA/ASIC options

“Bitstream” timing closure

TierFPGA

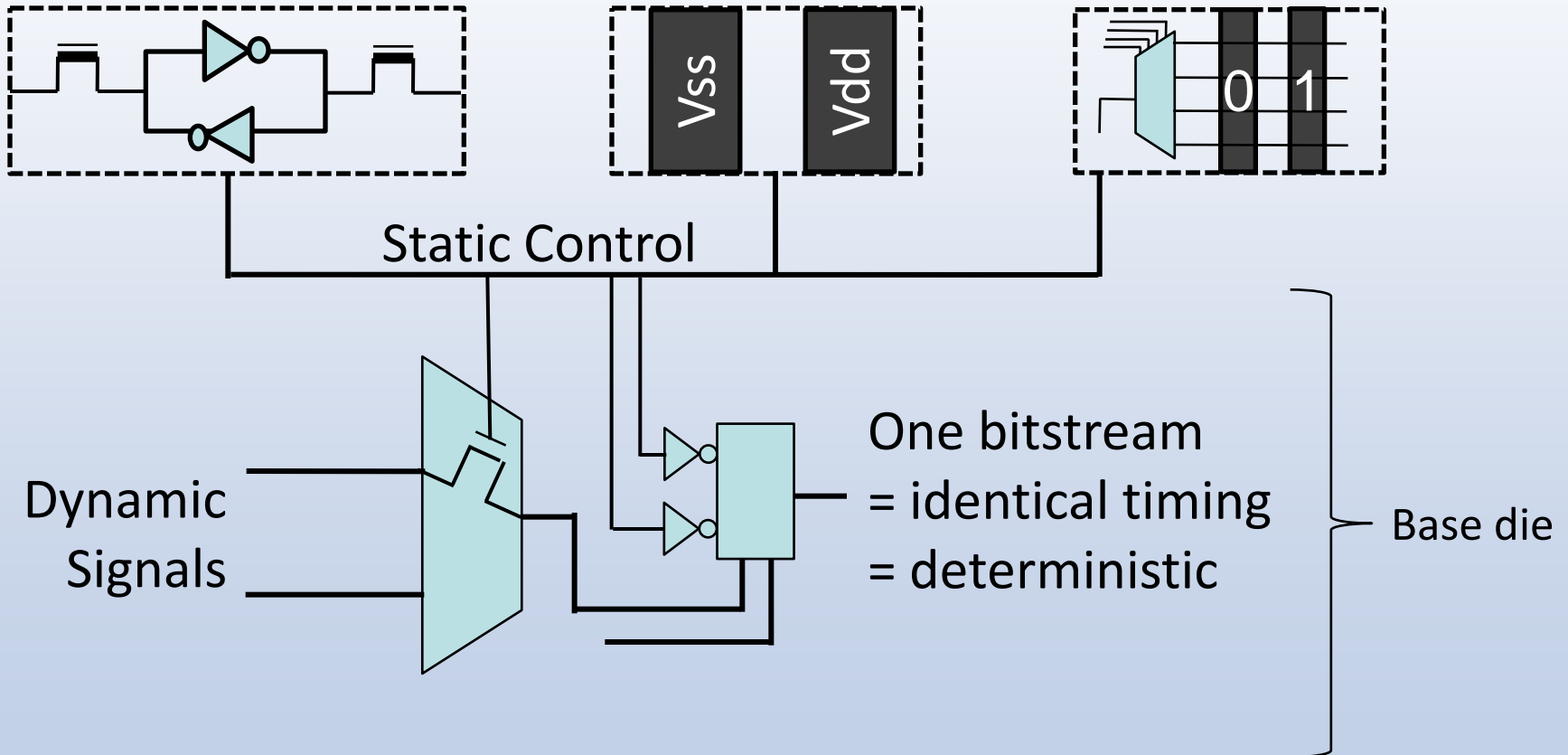
- TFT SRAM

TierASIC

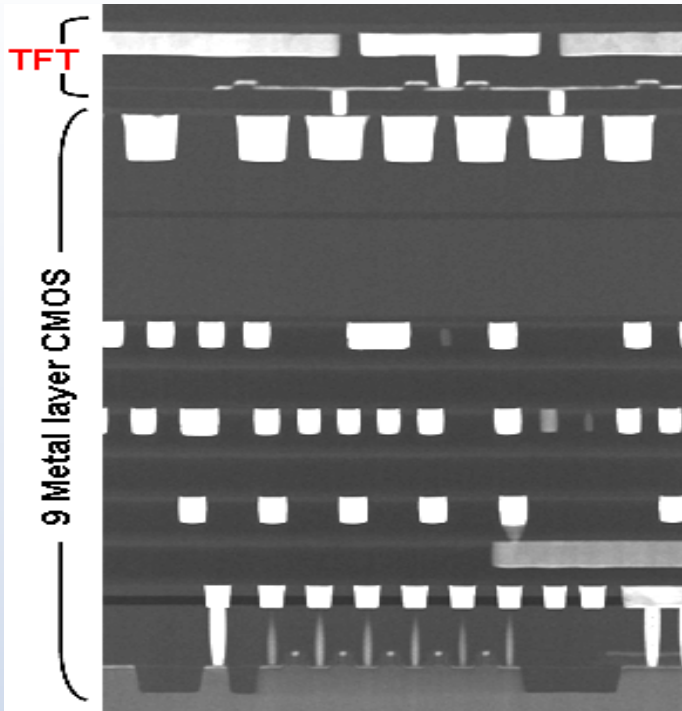
- Metal ROM

MultiASIC™

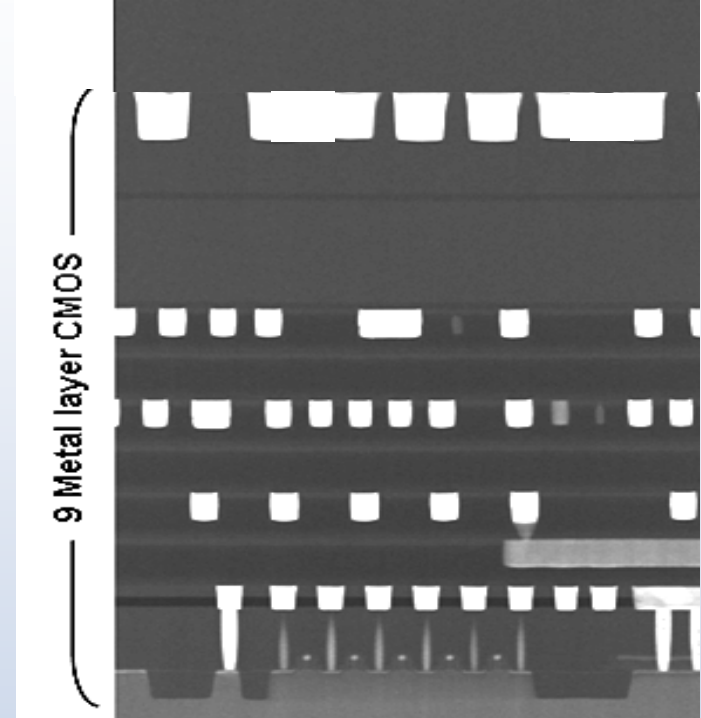
- TFT MUX



Monolithic process

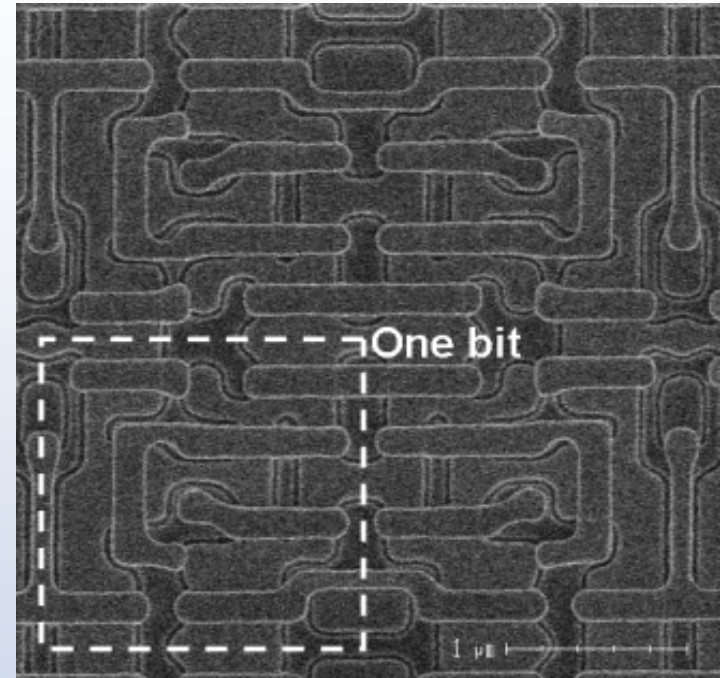
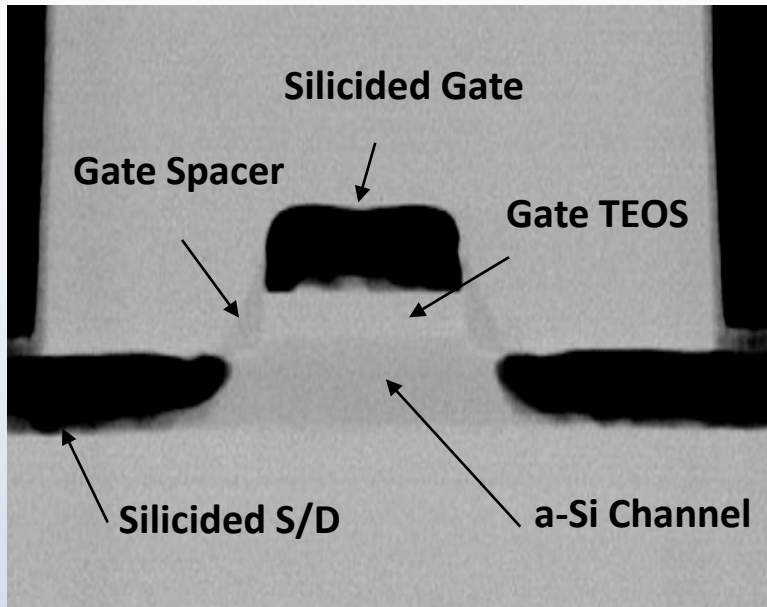


- TFT SRAM/MUX over CMOS
 - FPGA fabric / FPGA tools
 - Temperature < 400 °C



- Metal ROM over CMOS
 - FPGA fabric / FPGA tools
 - “Bitstream” custom M9

Thin-film-transistors (TFT)

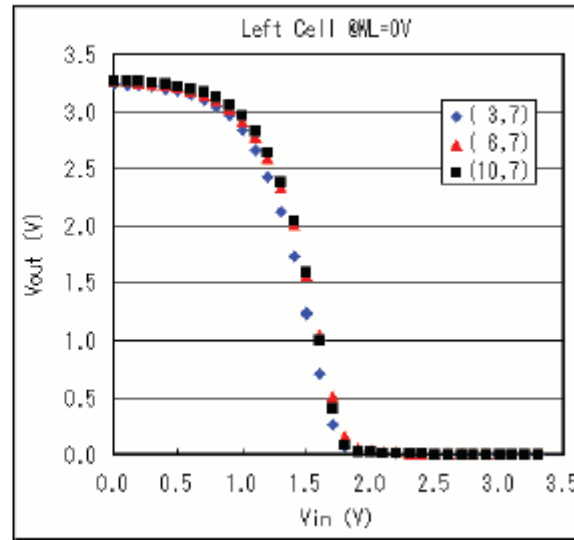
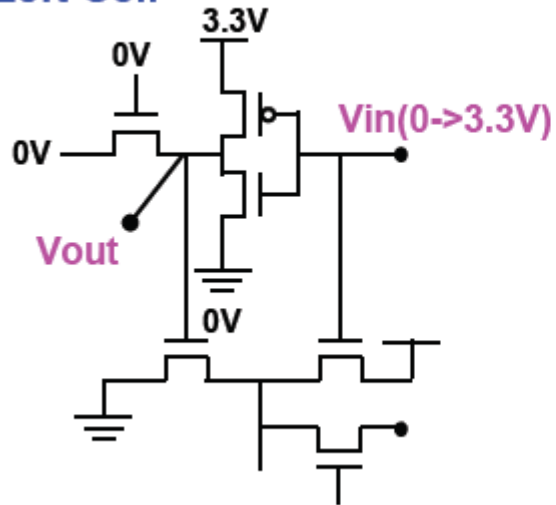


- N/P thin-film transistors
 - Majority carrier
 - Accumulation mode

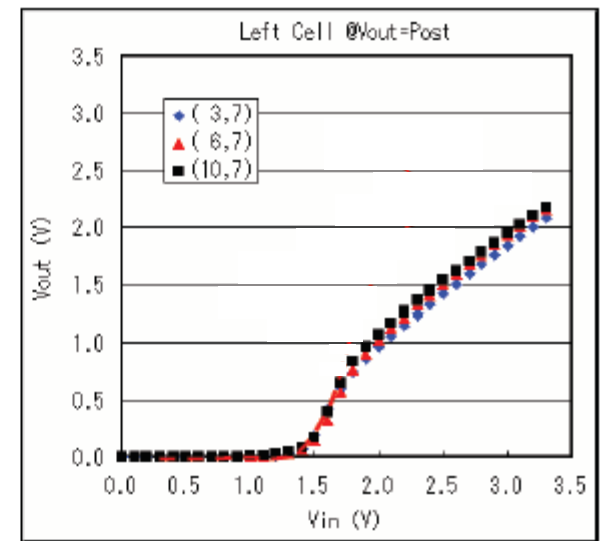
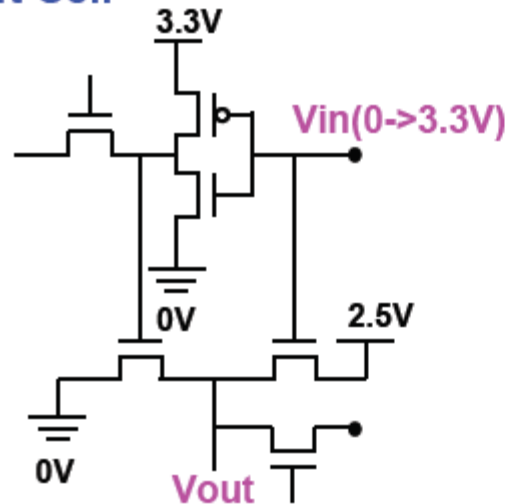
- 9-TFT SRAM cell
 - $< 10\mu\text{W}$ static / 10^6 bits
 - $I_{\text{ON}} / I_{\text{OFF}}$ stable & durable

TFT SRAM latches

Left Cell

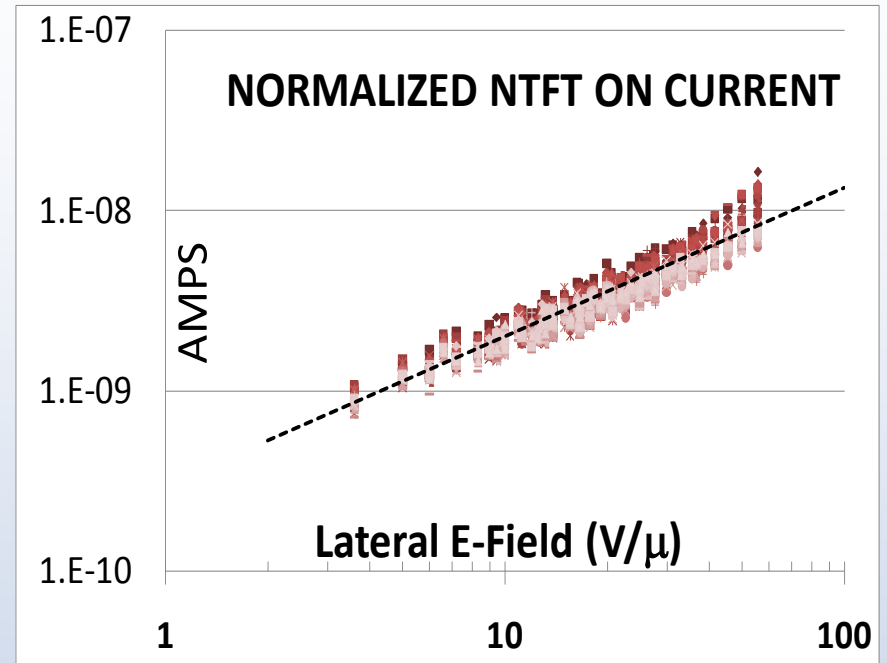
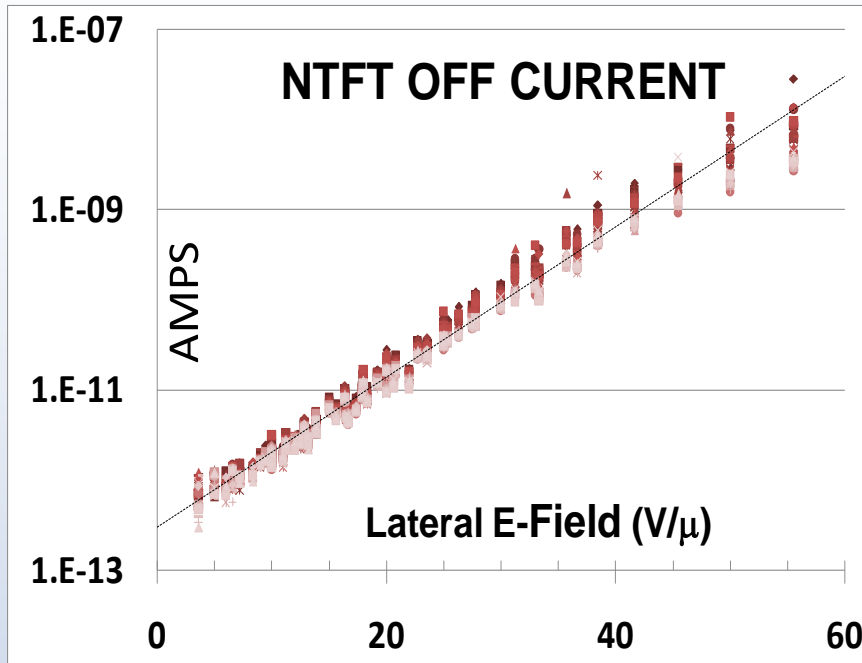


Left Cell



- Static circuits
- V_T not critical
- Low power

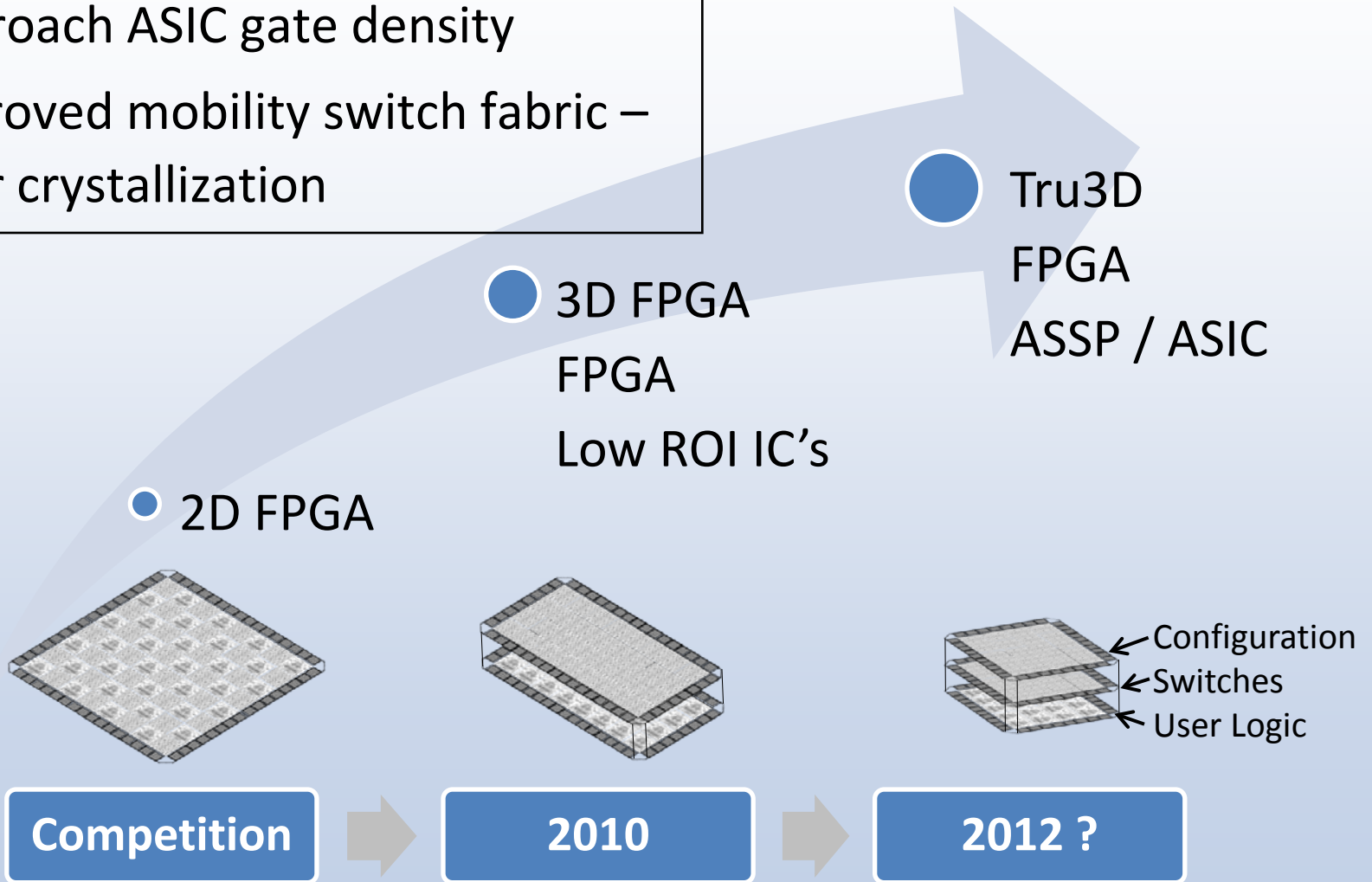
E-field scalable



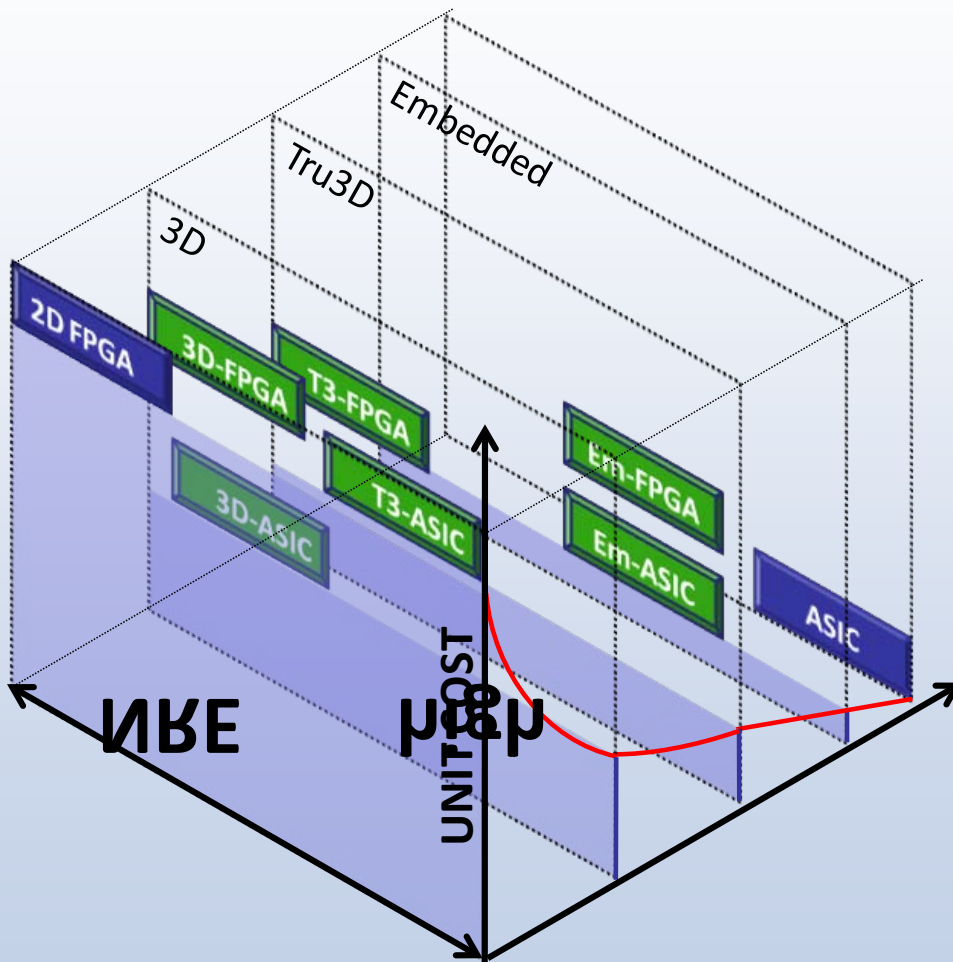
- 90nm CMOS – TFTs operate at 3.3V
- 45nm CMOS – TFTs operate at 1.8V
- Scale with CMOS

Improving gate density

- Approach ASIC gate density
- Improved mobility switch fabric – laser crystallization

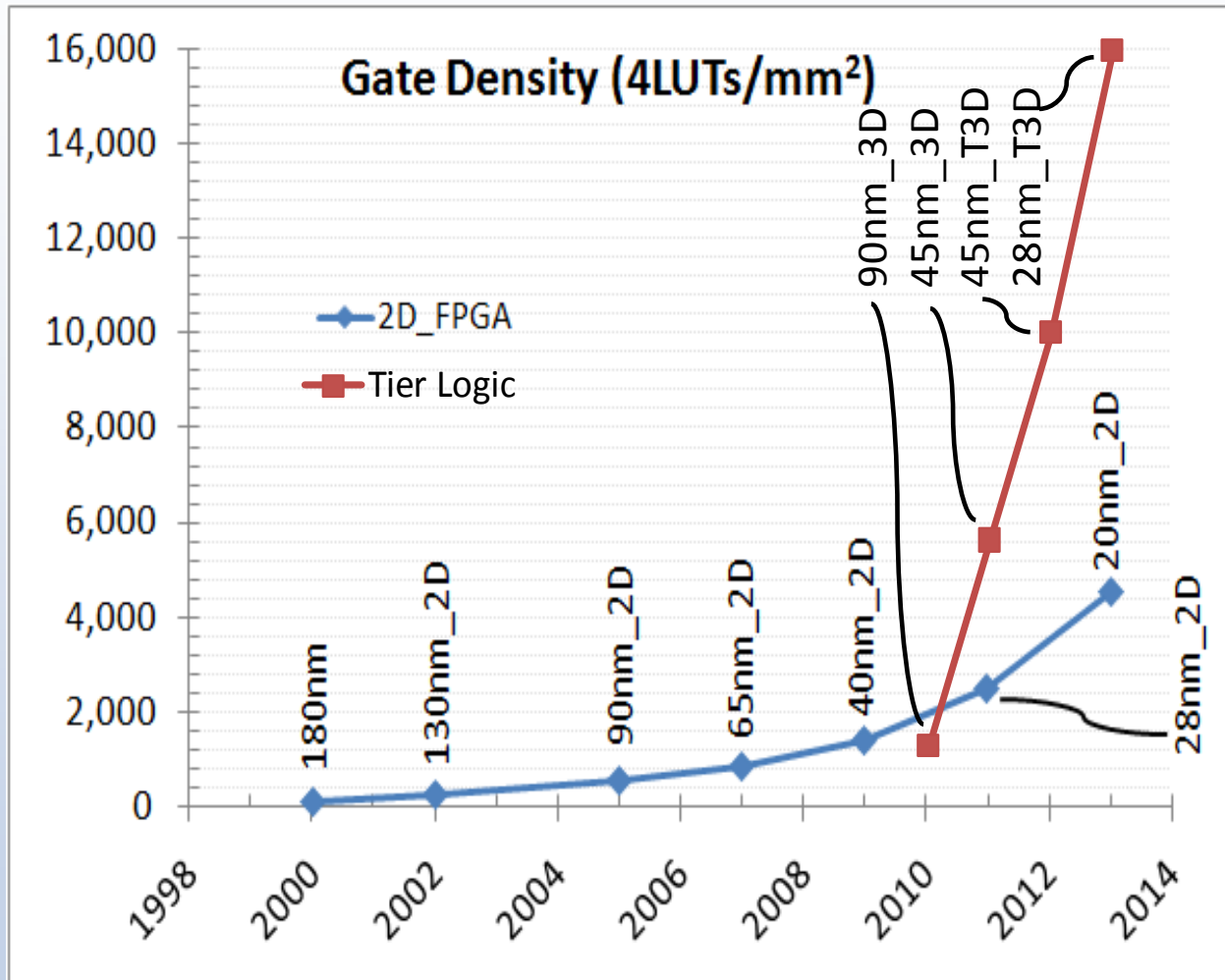


Competitive evolution



- Multi-faceted technology evolution
 - 3.5x 3D FPGA
 - 7x Tru3D
- Programmability – as needed – iterative
- Fixed function – when satisfied
- All future ICs will need programmability
- 56 issued patents

4LUT gate density



2D FPGA 4LUT density: follow Moore's Law

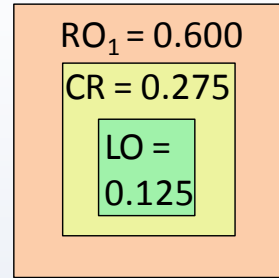
- 180nm = 110/mm² (FY2000)
- 20nm ~ 4500/mm² (FY2013)
- 6 nodes ~ 40x

3D gives higher 4LUTs

- 28 nm = 16k /mm² (FY2013)

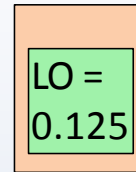
Routing architecture

Area:
 CR = CRAM
 LO = Logic
 RO = Routing



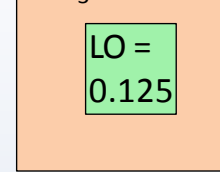
area=1

$RO_2 = 0.4 * e$

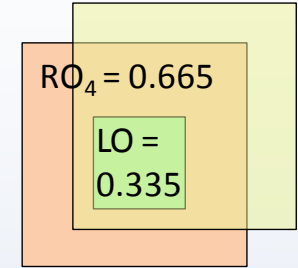


area=e

$RO_3 = 0.60 * f$



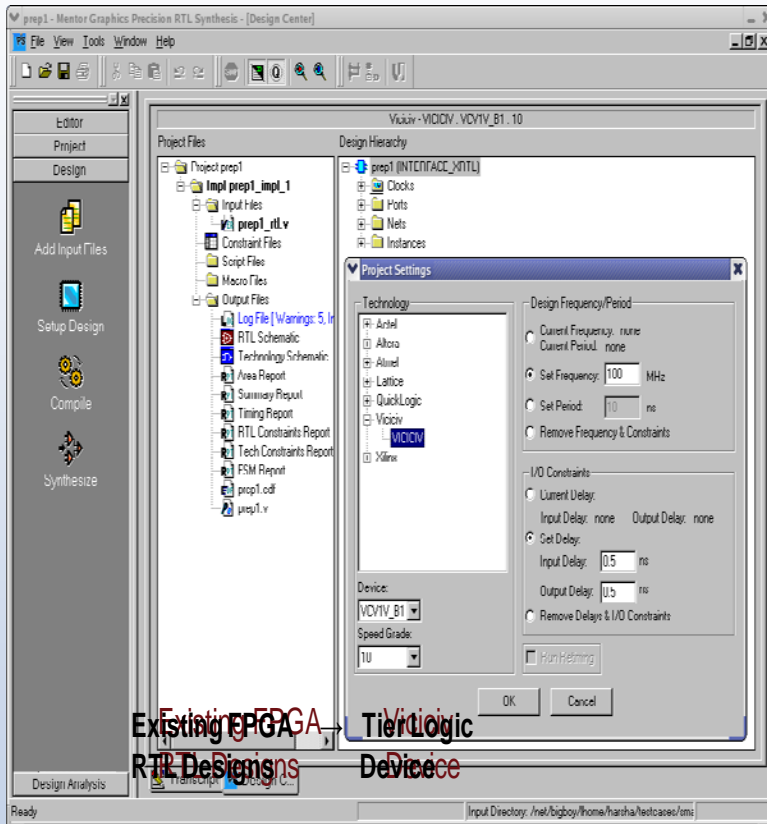
area=f



area=1

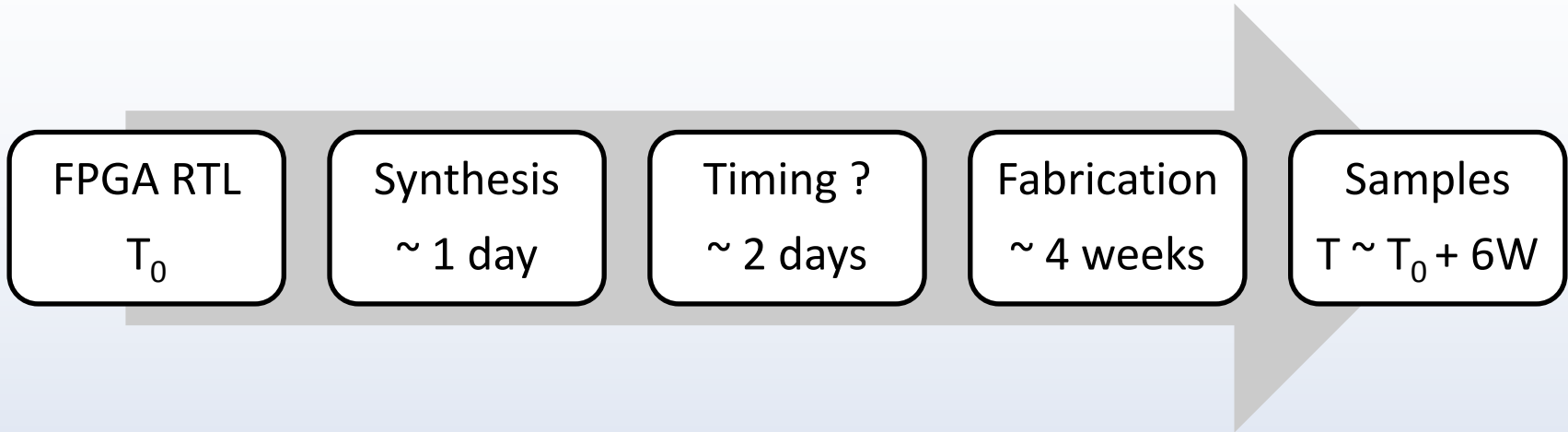
ARCHITECTURE	2D FPGA	ASIC	2D FPGA (No CR)	3D FPGA (3D CR)
Logic cell area	1	$e = 0.208$	$f = 0.313$	$g = 1$
Wires / area	N	N	N	N
RO per wire	$0.6 / N$	$0.4 / N$	$0.6 / N$	$0.665 / N$
LO area	0.125	0.125	0.125	0.335
RO area	$RO_1 = 0.6$	$RO_2 = 0.4 * e$	$RO_3 = 0.6 * f$	$RO_4 = 0.665$
Area (RO+LO+CR)	$1 = CR + LO + RO_1$	$e = LO + RO_2$	$f = LO + RO_3$	$g = LO + RO_4$
LO ratio to 2D	1.0	4.8	3.2	2.7
LO Efficiency	1	6	1	1.4
User LO / area	1	28.8	3.2	3.8

Unified tools



- FPGA RTL design entry
 - Mentor “Precision” synthesis
 - Tier Logic “Mobius” P&R
- One tool – one placement
 - “Bitstream” for FPGA
 - “M9 mask” for ASIC
- Excellent quality of results
- Combining tools, design & process

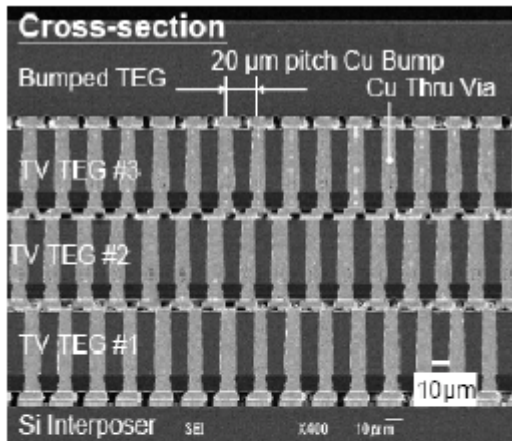
FPGA design for ASICs



- FPGA verified RTL
- Standard front end tools
 - No re-design
 - TierFPGA to re-verify (if necessary)
 - Pin compatible TierASICs (6 weeks + \$50k)

Die stack vs. monolithic

Reference: 3rd Stanford and Tohoku Universities joint Open Workshop on 3D Transistors and its Applications December 2009



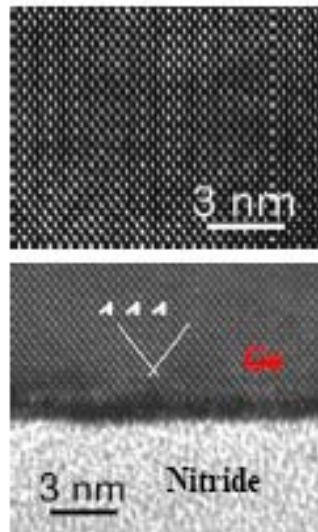
Source : NEC Corporation

Limits the vertical interconnect density to $10^5 - 10^6 / \text{mm}^2$

K. W. Guarini et al., *IEDM 2002*

S Gupta et al., *VMIC 2005*

A. W. Topol et al., *IEDM 2005*



Monolithic Stacking

Vertical interconnect pitch $> 200 \text{ nm}$

Vertical interconnect density $\sim 2\text{B}/\text{cm}^2$

Connect at device level

- FPGA's need $> 90\%$ area for wires
- 40nm 2D CRAM bit density $\sim 90\text{M} / \text{cm}^2$
 - Requirement for Via $> 1\text{B} / \text{cm}^2$

Summary

- Unified IC design for FPGA & ASIC
 - Beyond process scaling
 - “Bitstream” concept to IC design
- Worlds first monolithic 3D FPGA
 - Same “netlist / placement / base-die” → 3D ASIC
 - Fine grain for logic & course grain for routing
- Augment programmability to ASIC density
 - High mobility 3D nTFT switches

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