

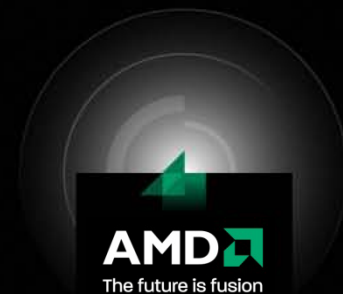


"Bobcat"

AMD's New Low Power x86 Core Architecture

Brad Burgess, AMD Fellow
Chief Architect / Bobcat Core

August 24, 2010



Two x86 Cores Tuned for Target Markets



"Bulldozer"

Performance &
Scalability



Mainstream Client and Server Markets



"Bobcat"

Flexible, Low
Power & Small

Low Power
Markets



Small
Die Area

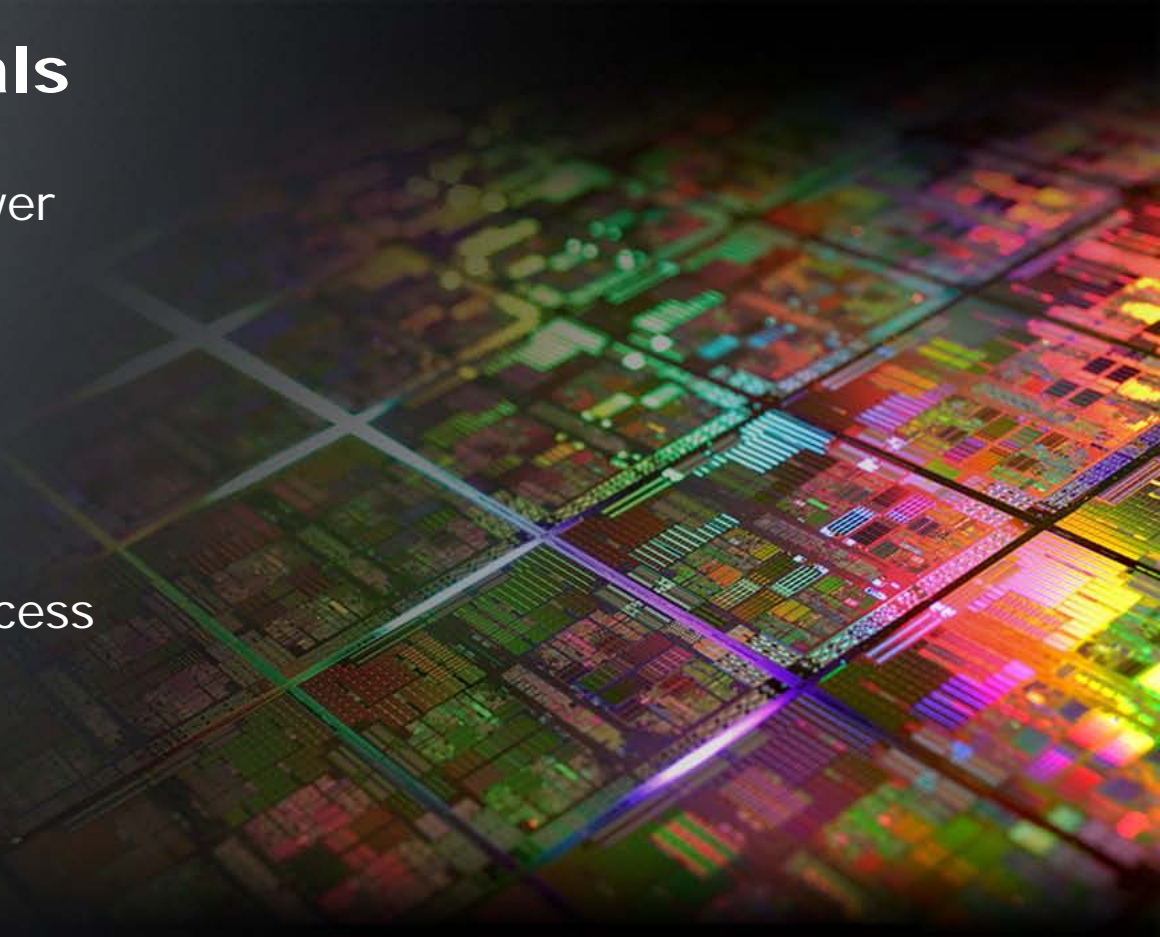


Cloud Clients
Optimized



Bobcat Design Goals

- A small, efficient, low power x86 core
- Excellent performance
- Synthesizable with small number of custom arrays
- Easily Portable across process technologies



Feature Set

- 64-bit AMD64 x86 ISA
- SIMD extensions: SSE1, SSE2, SSE3, SSSE3, SSE4A
- Virtualization
- Support for misaligned 128-bit data types
- Instruction Based Sampling (for dynamic optimization)
- C6 (with integrated power gating)



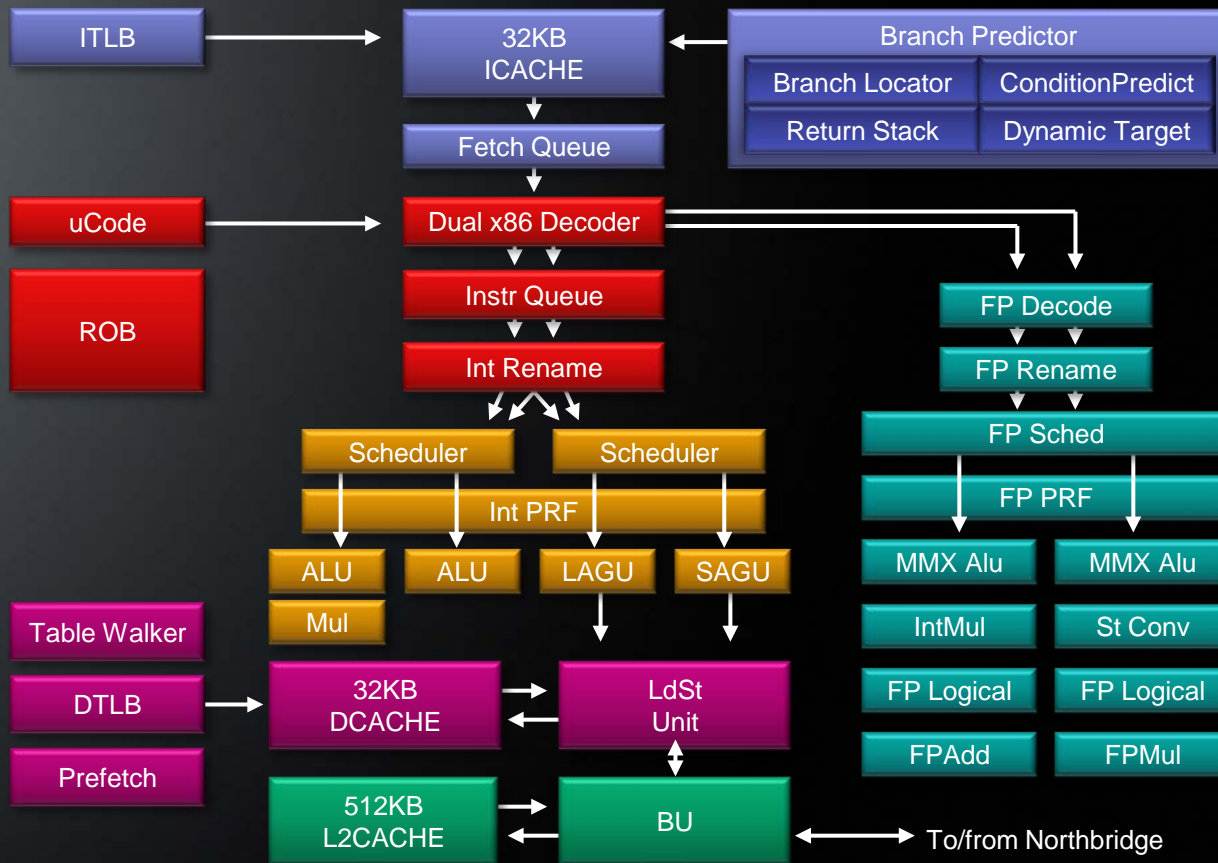
Micro-architecture Overview

- Dual x86 instruction decode
- Out-of-Order instruction execution
- Dual COP retirement
- Complex microOPs
- State of the art branch prediction
- Aggressive OOO load/store engine w/ hazard prediction
- Advanced Virtualization w/ nested page tables, ASIDs and world switch acceleration
- Low power C6 state w/ core level power gating and state save acceleration



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Micro-Architecture

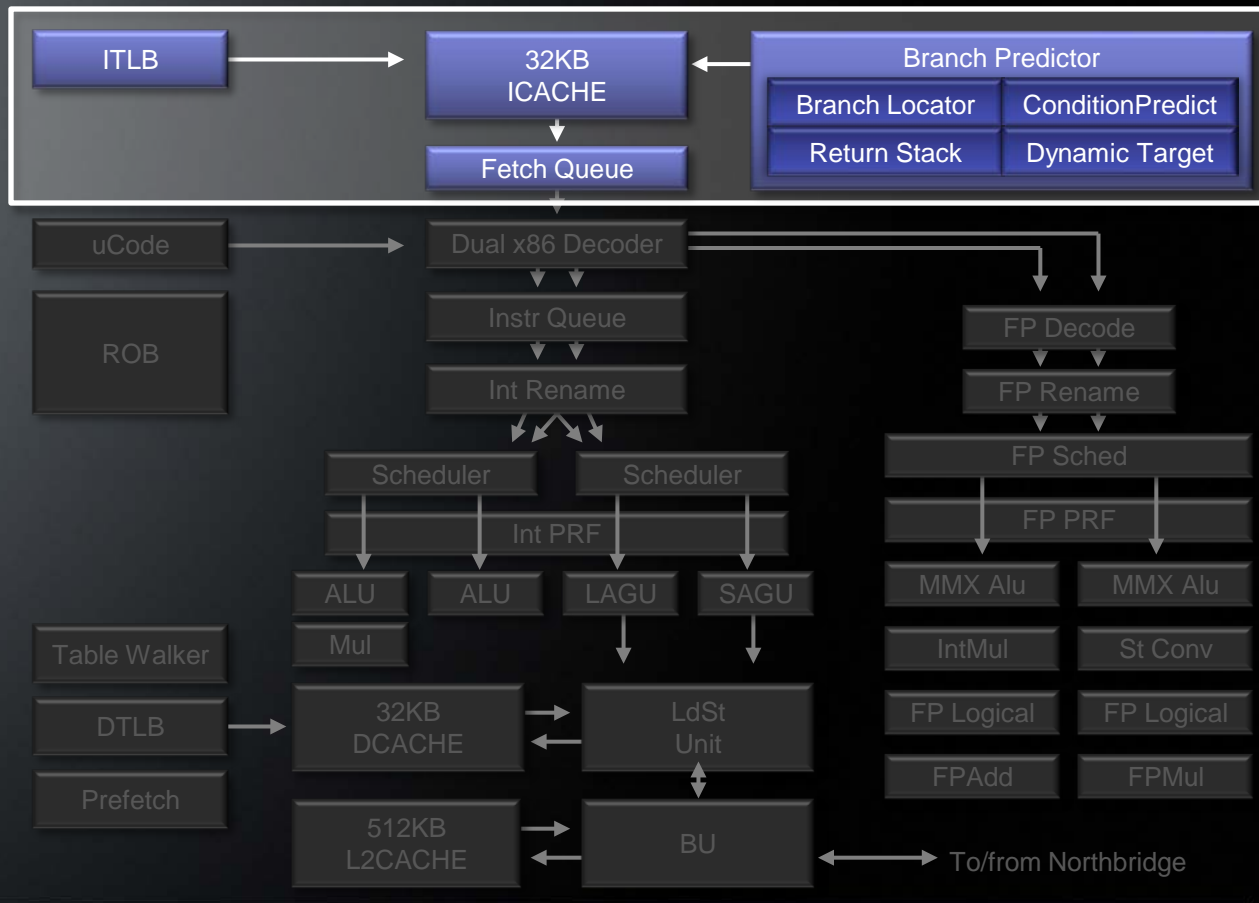


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Micro-Architecture

Icache

- 32Kbyte
- 2-way set associative
- 64-byte line
- Parity Protected
- 512/8 entry ITLB (4k/2m)
- Fetch up to 32-bytes/cycle

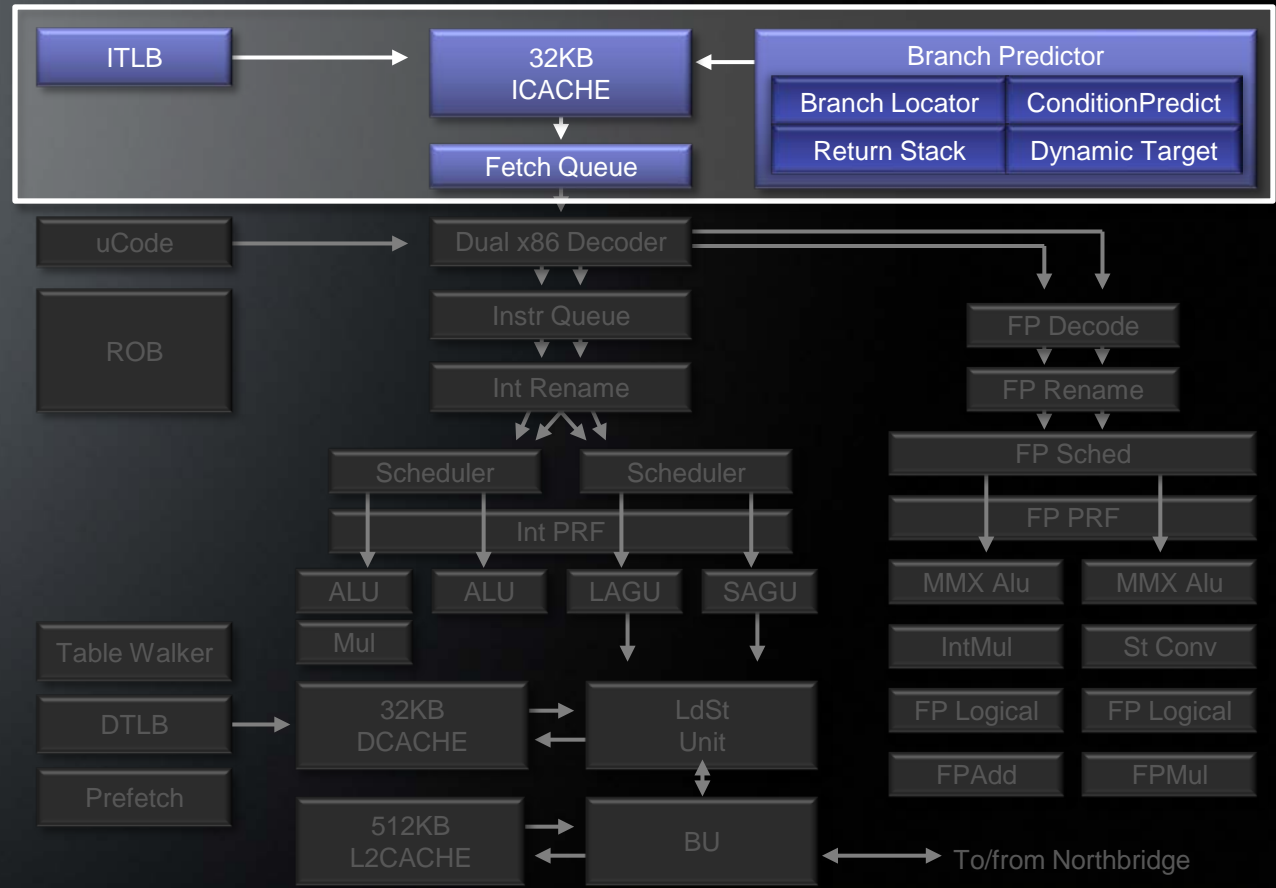


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Micro-Architecture

Branch Predictor:

- Predicts up to two branches per cycle
- Remembers branch instruction locations
- Return Stack Address Predictor
- Indirect Dynamic Address Predictor
- State of the Art condition Predictor
- Only necessary structures are clocked

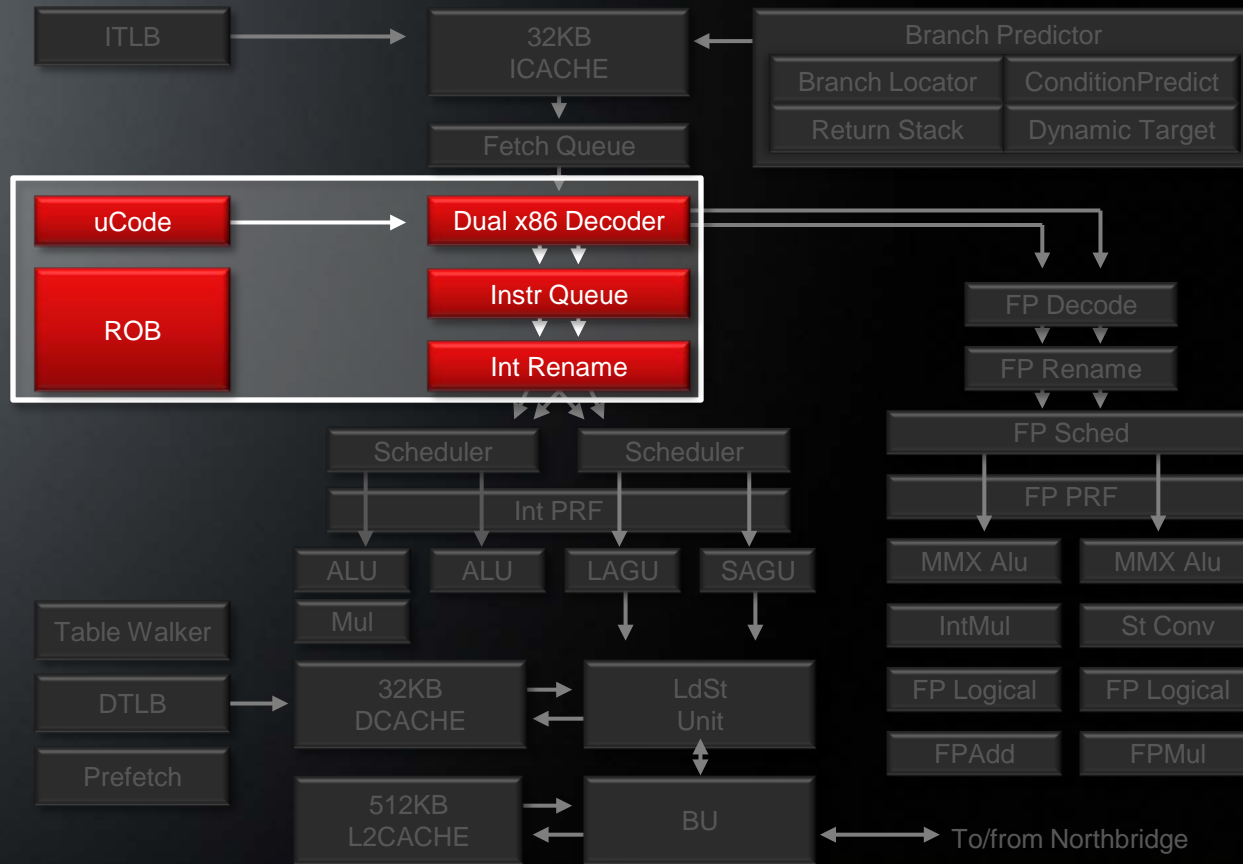


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Micro-Architecture

Dual x86 Decoder:

- Scans up to 22 bytes
- Decodes up to two x86 instructions per cycle
- The decoder can directly map 89% of x86 instructions to a single microOp, an additional 10% to a pair of microOps, and more complicated x86 instructions (<1%) are microcoded. (Dynamic Instruction Counts)

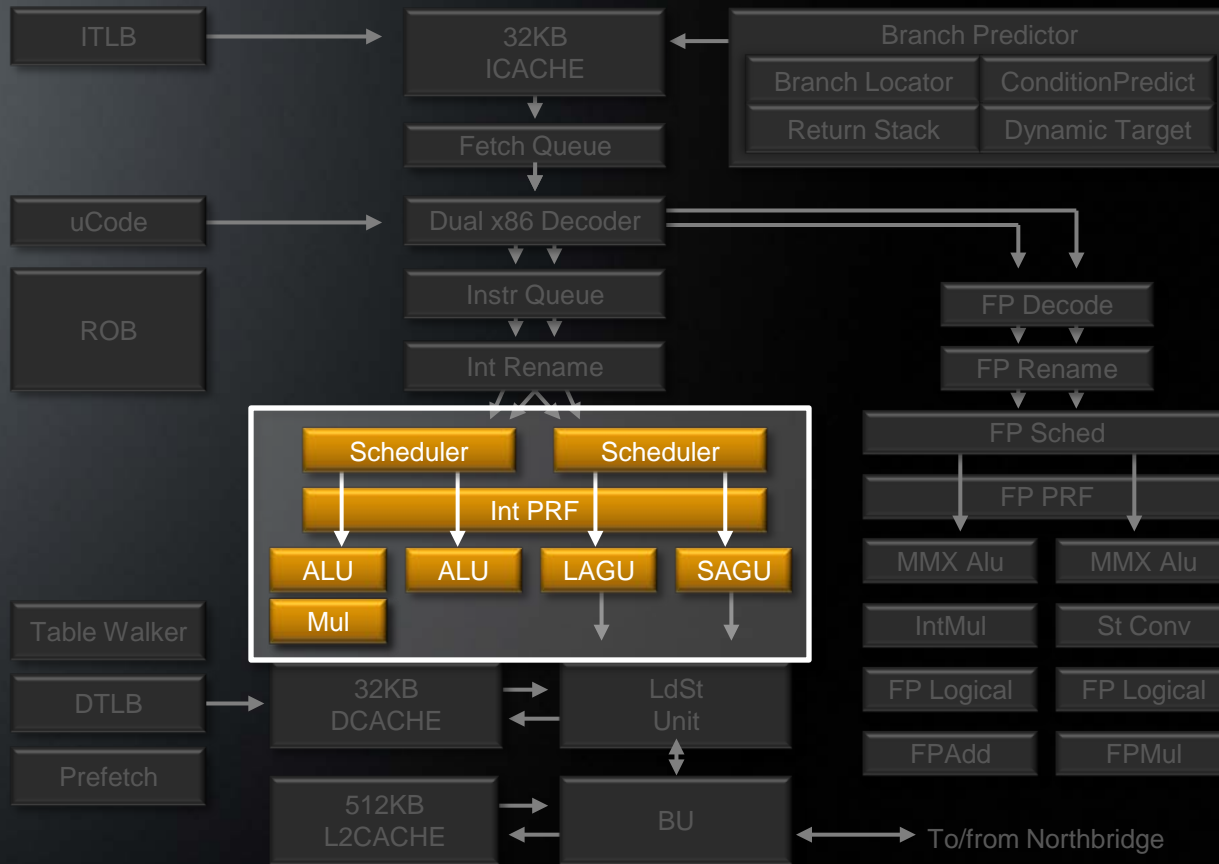


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Micro-Architecture

Integer Execution:

- A dual port integer scheduler feeds two ALUs
- A dual port address scheduler feeds a load address unit, and a store address unit.
- Physical Register File uses maps and pointers to reduce power by minimizing data copying/movement.

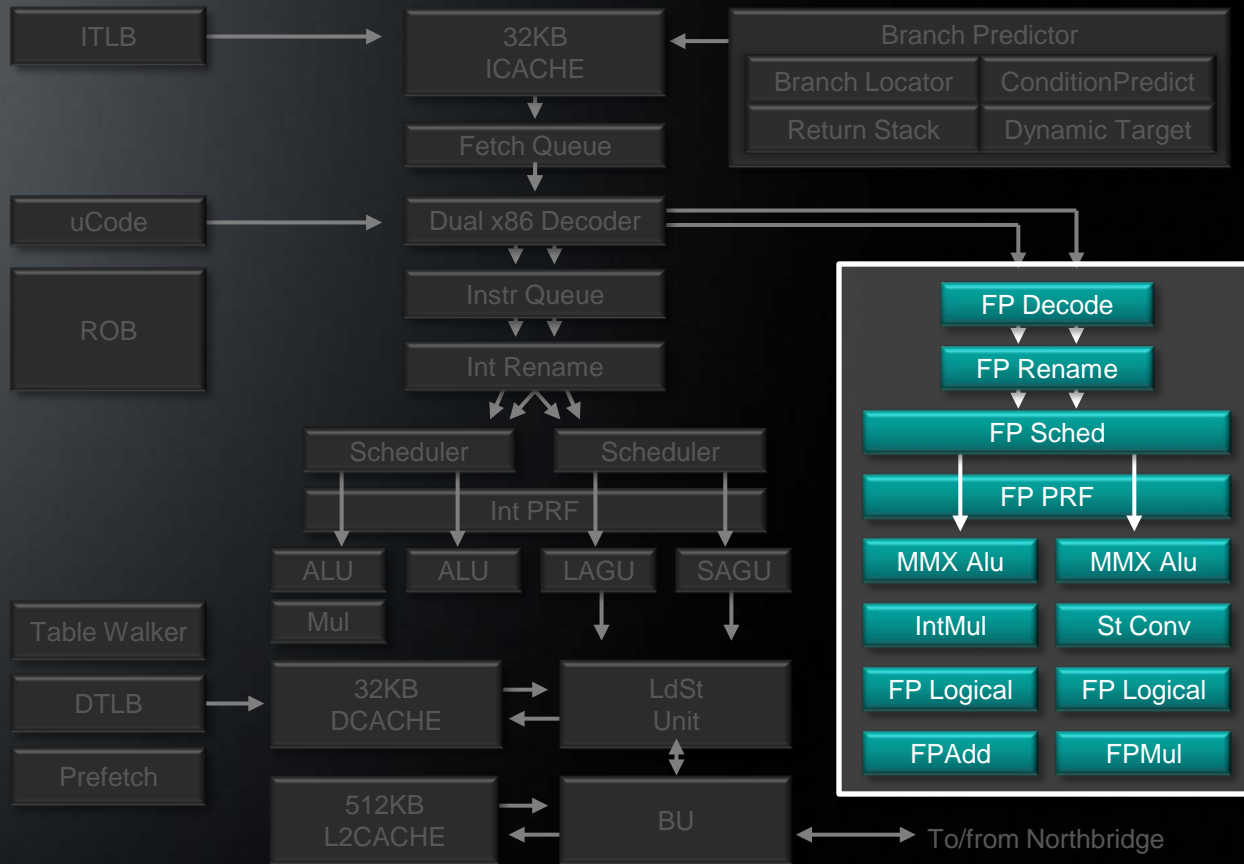


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Micro-Architecture

Floating Point Unit:

- A centralized FP scheduler feeds two 64-bit FP execution stacks
- MMX and Logical units are replicated in both stacks
- The FP Mul Unit can perform two SP multiplies per cycle
- The FP Add Unit can perform two SP additions per cycle
- A physical register file is used to reduce power

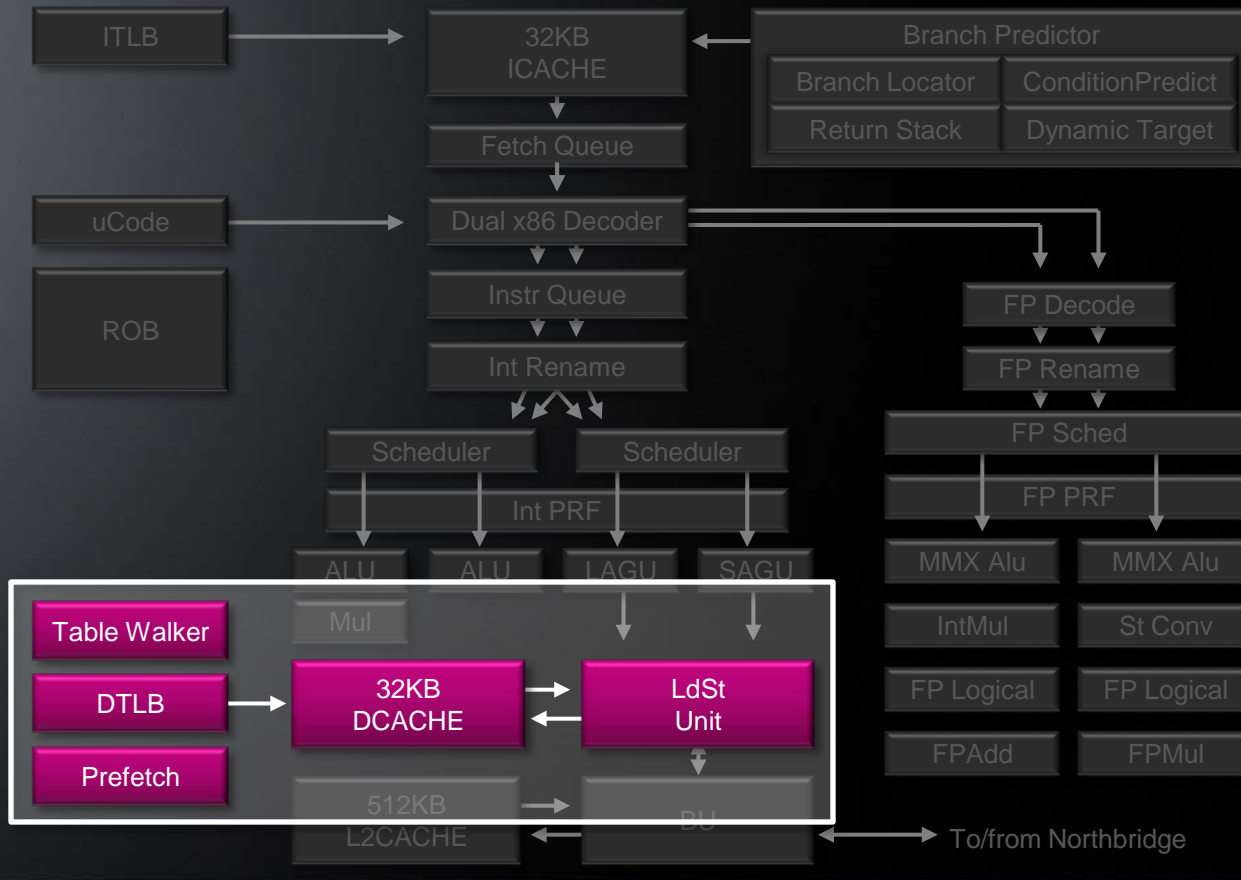


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Micro-Architecture

Data Cache:

- 32-Kbyte
- 8-way set associative
- 64-byte line
- Parity Protected
- Copyback
- 40/8 entry L1DTLB (4k/2m)
- 512/64 entry L2DTLB (4k/2m)
- Advanced 8-stream prefetcher

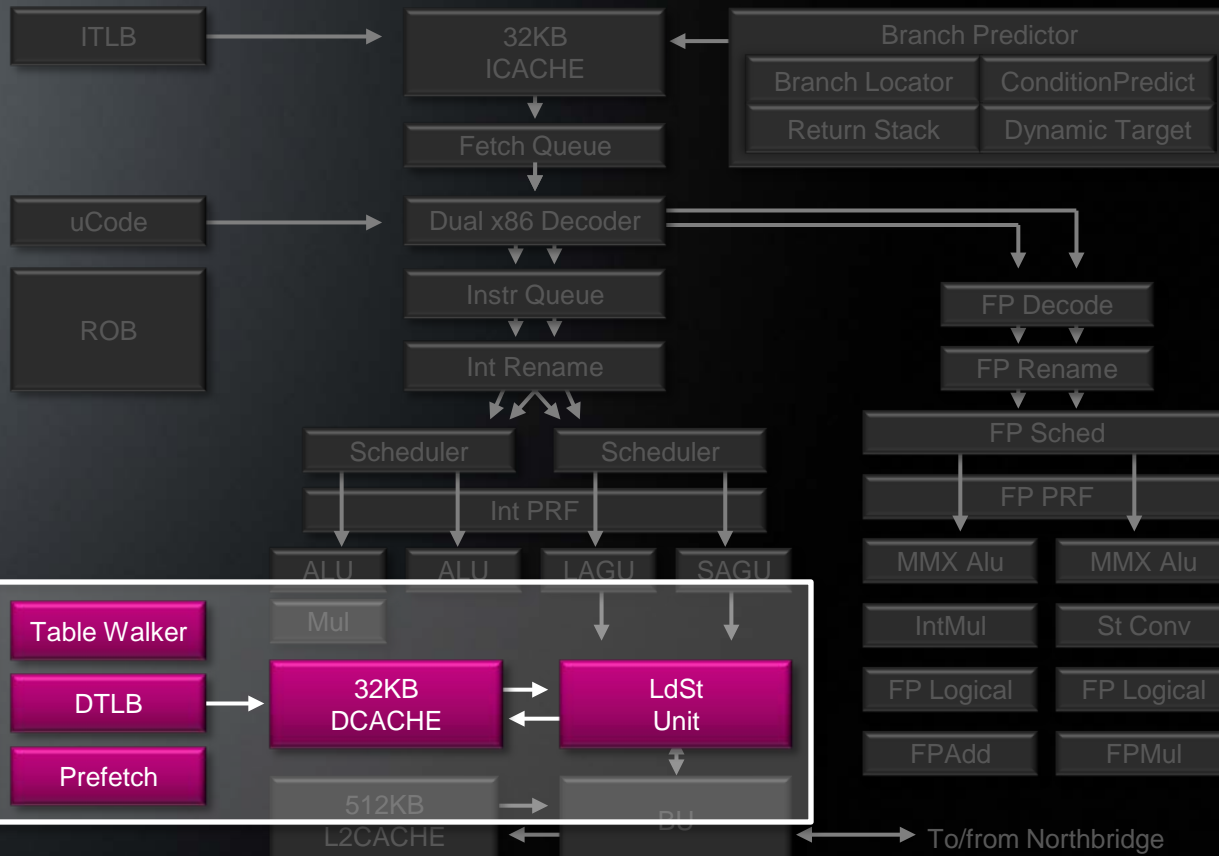


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Micro-Architecture

Out-of-Order Load Store Unit:

- Loads bypassing loads
- Loads bypassing stores
- Stores bypassing loads
- Bypass tracking and dependency correction
- Hazard predictor
- Fast store forwarding
- Fast critical word fill forwarding

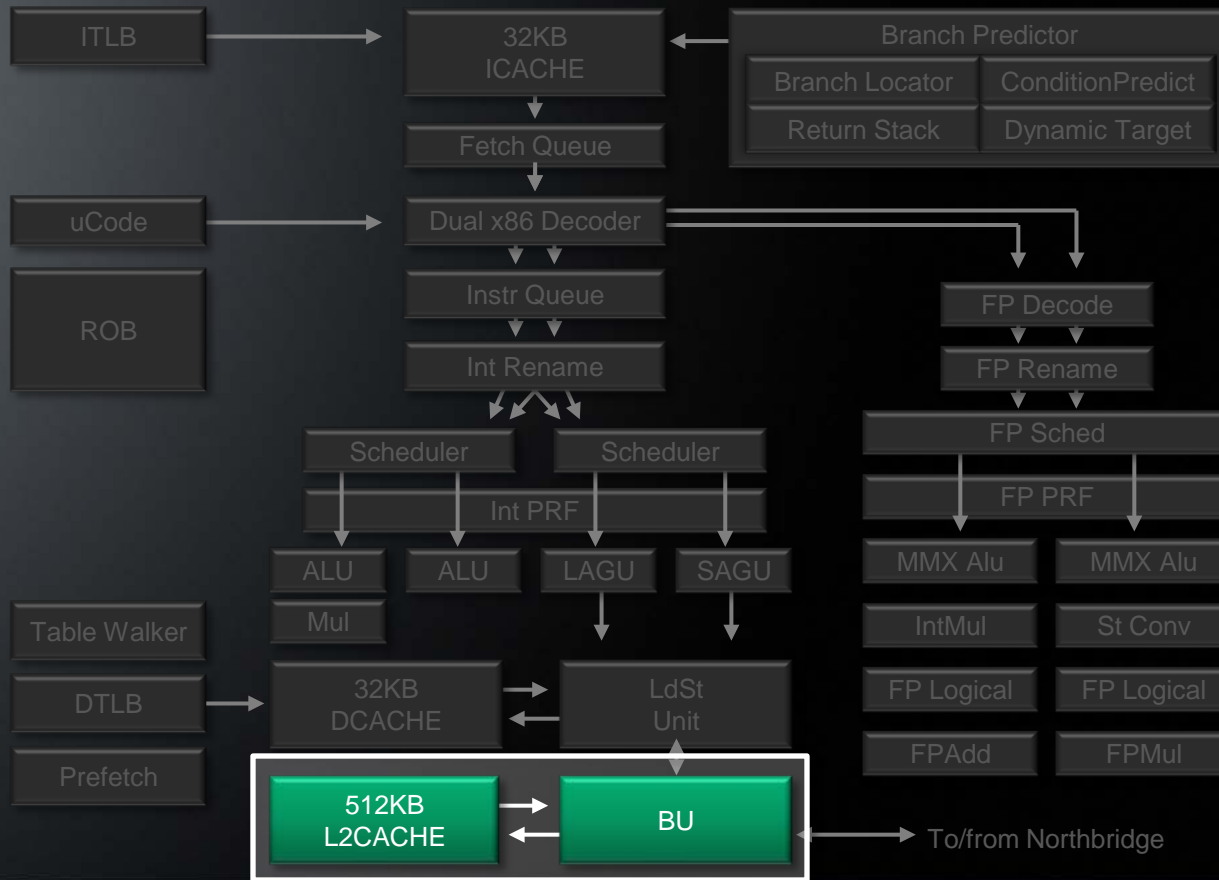


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Micro-Architecture

L2 Cache:

- 512Kbyte
- 16-way set associative
- 64 byte lines
- ECC Protected
- Half speed clocking for power reduction

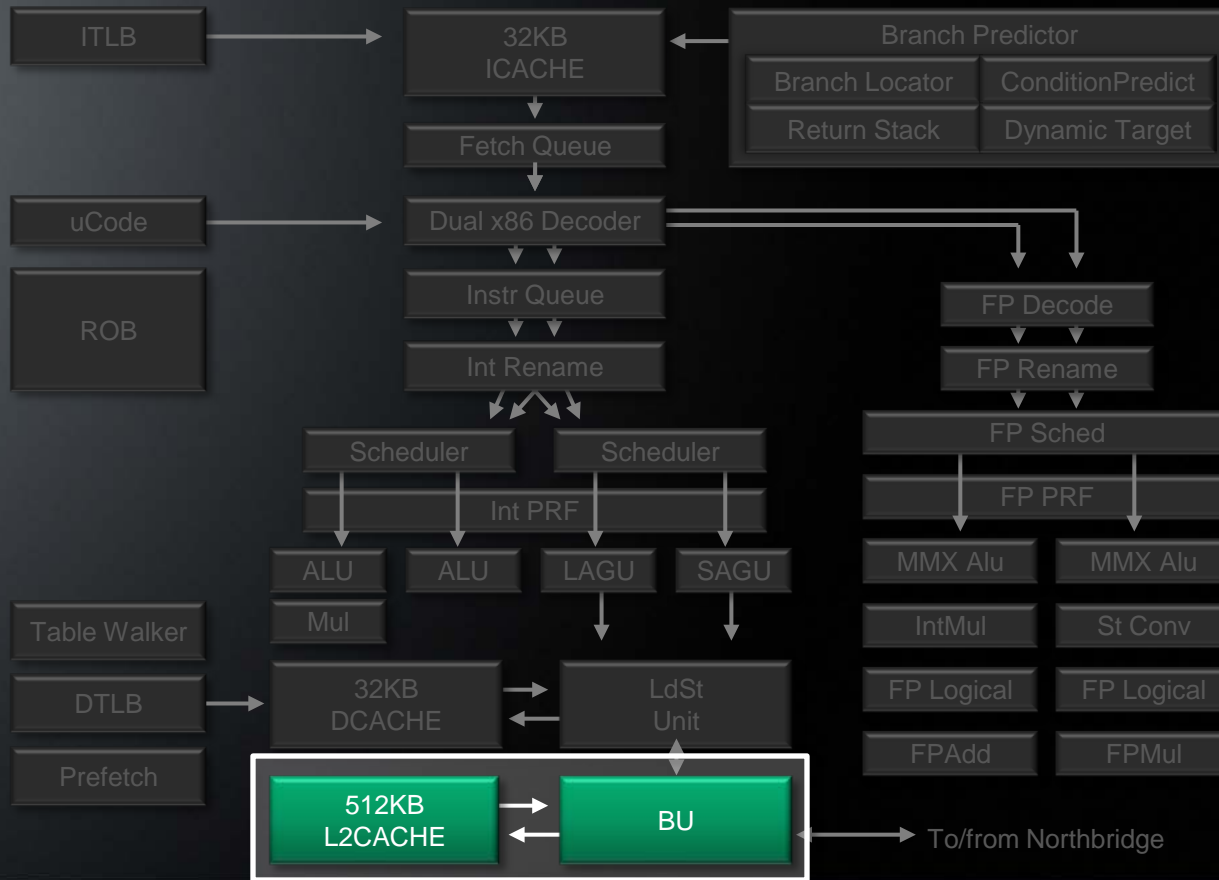


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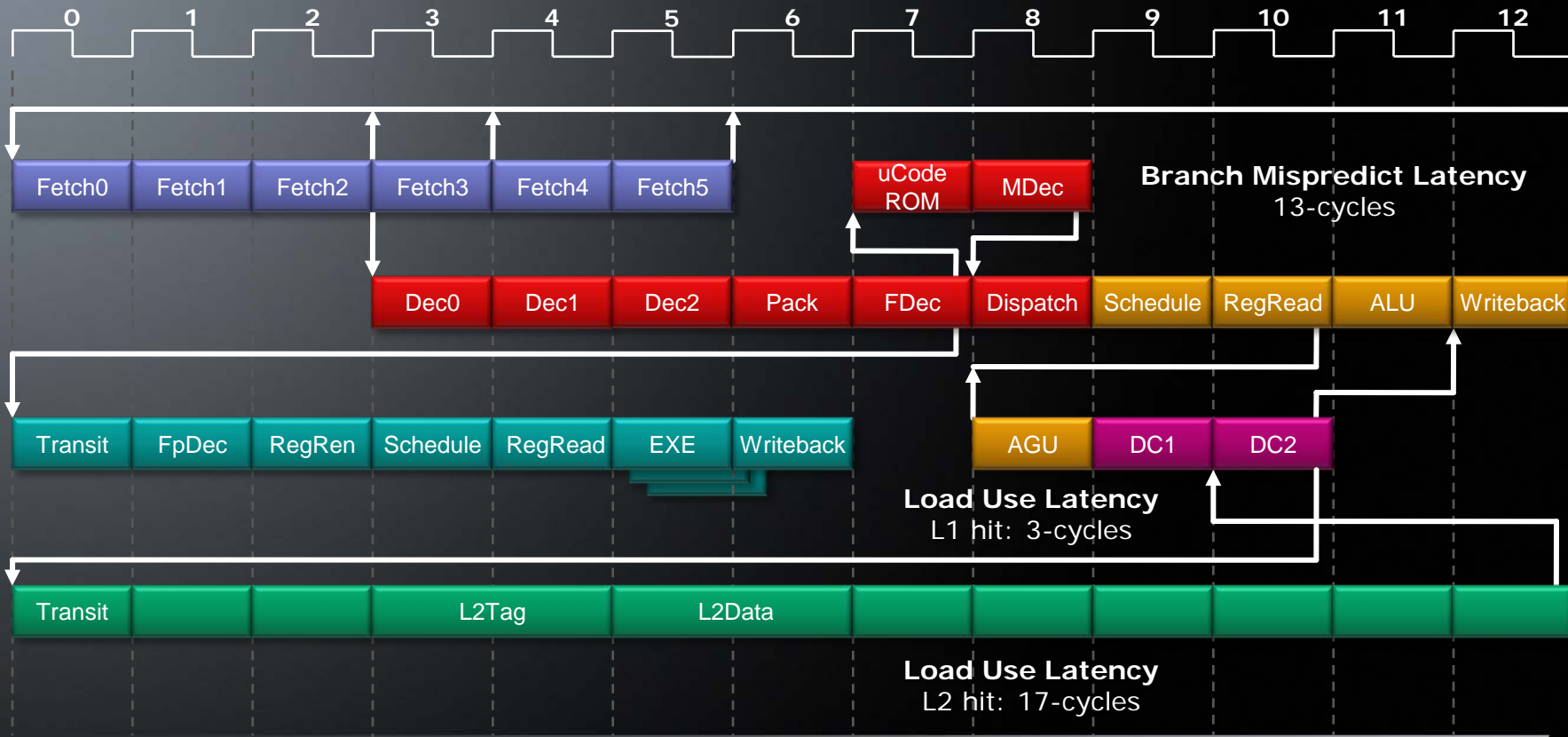
Micro-Architecture

Bus Unit:

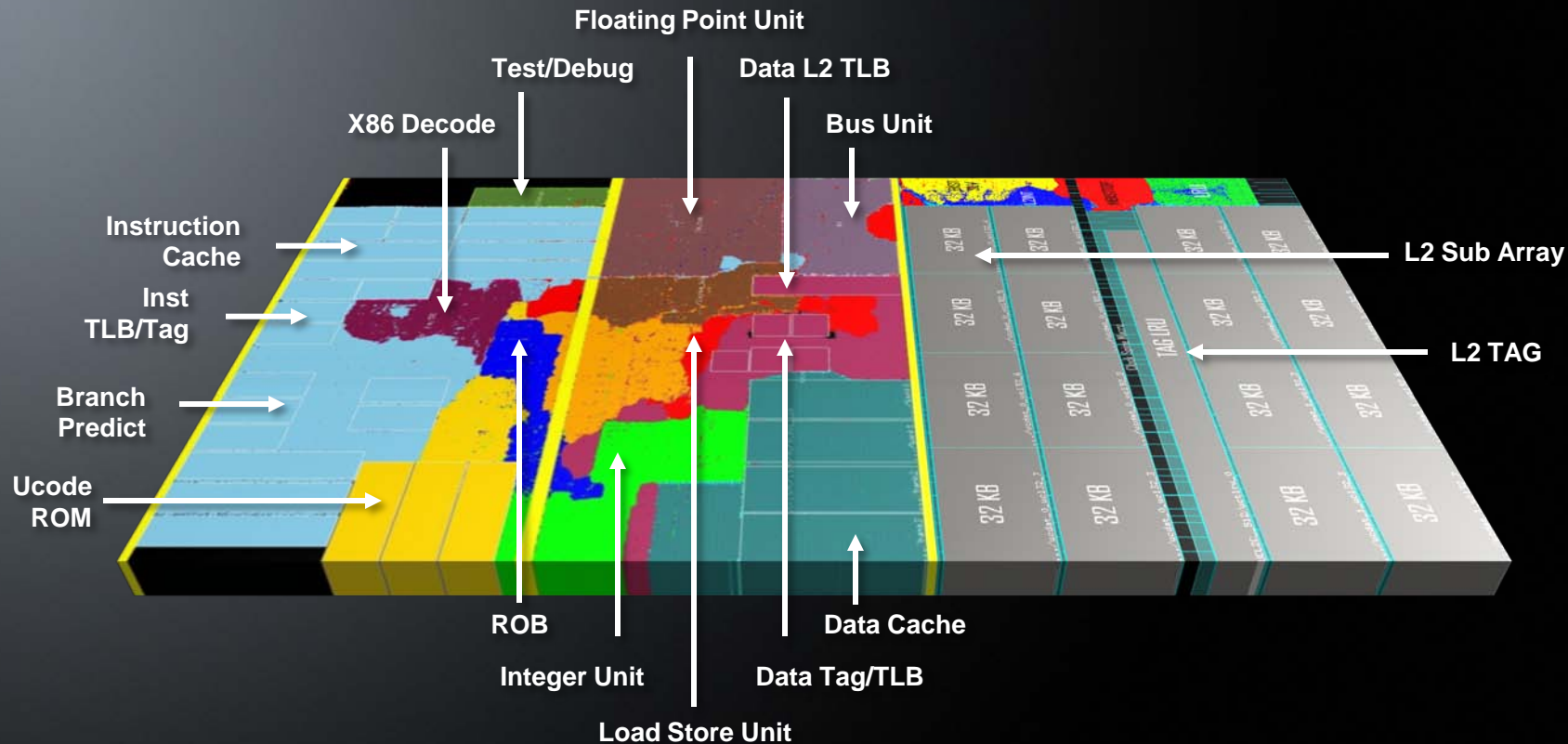
- 8-outstanding data accesses
- 2-outstanding fetch accesses
- Eviction Buffers
- Fill Buffers
- Write combining buffers
- Coherency management



Bobcat Pipeline



Core Floor Plan



Power Reduction

- Use of physical Register files
- Extensive use of non-shifting queues with pointers
- Fine grain clock gating
- Integrated Core Power Gating
- Only needed arrays are clocked
 - i.e. Dtag hit before Dcache read
 - Predicting the type of branch then clocking the appropriate predictor(s)
- Elimination of instruction marker bits in the Icache
- Finding the knee of the curve (scrutinize performance gains against power costs)
- Polishing speed paths to raise the Vt mix and reduce leakage



Bobcat Core Overview

Advanced Micro-architecture

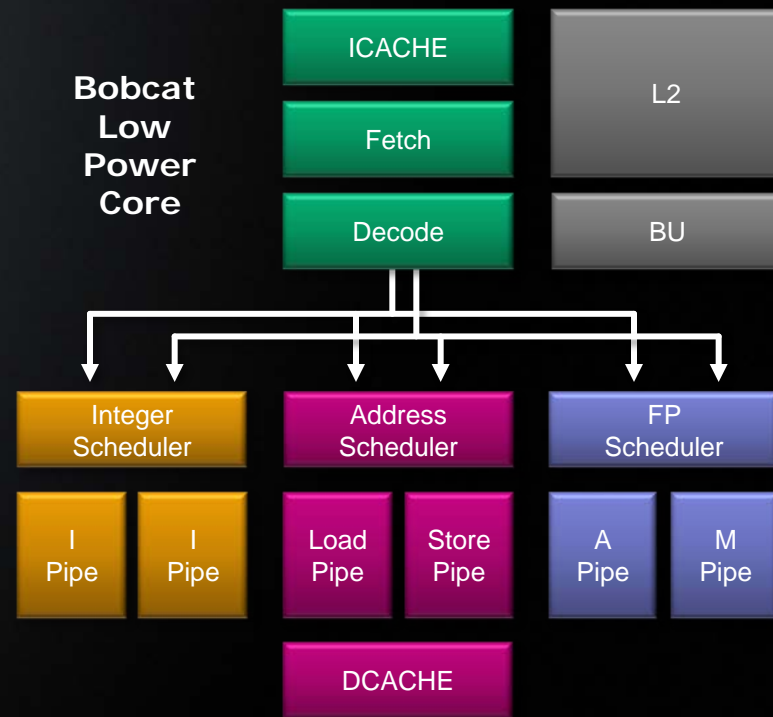
- Dual x86 Decode
- Advanced Branch Predictor
- Full OOO instruction execution
- Full OOO load/store engine
- High Performance Floating Point
- AMD64 64-bit ISA
- SSE1,2,3, SSSE3 ISA
- Secure Virtualization
- 32kb L1s, 512kb L2

Low Power Design

- Power Optimized Execution
- Micro-architecture that minimizes data movement and unnecessary reads
- Clock gating, Power gating
- System Low Power States

Small Core

- Area efficient balance of high performance and low power



Summary

- Estimated 90% of the performance of today's mainstream notebook CPU in half the area*
- Sub-one watt capable
- Highly portable across designs and manufacturing technologies

