Hummingbird: A Low-Cost Superscalar PA-RISC Processor

Stephen Undy
Hewlett-Packard
Hot Chips V

Presentation Outline

- Introduction
- Design Goals
- Processor Overview
- Cost Reduction
- Performance
- Scalability
- Power Reduction and Test
- Summary
Design Goals

- Minimize System Cost
- Meet or Exceed Current Mid-Range Workstation Performance in an Entry-Level System
  - Integer
  - Graphics
  - Multimedia
- Scalability
- Low Power Consumption
- Fully Compliant with PA-RISC Architecture
- Design for Manufacturability

Processor General Features

- Core Technologies and Features From PA7100
- High Integration
  - Floating Point and Integer Processors
  - On-chip Instruction Cache
  - Off-chip Cache Controller
  - Memory and I/O Controller
- 2-Way Superscalar
- 2 Integer ALUs
- Architectural Extensions
Architectural Features

- Support for Little-Endian Processes
  - PC Emulation and Other Software
- Support for Uncacheable Memory Pages
  - Enhances Performance of I/O Subsystems
- Support for Multimedia Processing
  - Improves Most Multimedia Applications
  - Addition / Subtraction with Saturation
  - Arithmetic Averaging
  - Shift-and-Add for Multiplication by Constant
  - Pixels, Audio Samples, Text
  - 4X Speed Up

Technology

- HP's CMOS26B Process
  - 0.8 micron FET's
  - 3-level Metal Interconnect
- 0-75+ MHz
- 900,000 Transistors
- 14mm x 14mm Die Size
- 432 Pin Cost-Reduced PGA
  - 1.8" x 1.8"
  - 50 mil Interstitial Pin-Grid
  - High-Speed Operation w/o Bypass Caps
- 5V Vdd, TTL Compatible I/O Levels
System Block Diagram

Hummingbird (PA7100LC)

Memory and I/O Interface

Level 1 ICache

TLB

FP Unit

Integer Unit #1

Integer Unit #2

External Cache Interface

Hewlett Packard
Cache Organization

- Internal:
  - Level 1 ICache
  - Instruction RPN
  - TLB

- External:
  - Level 2 ICache
  - DCache

Data addr → Instr addr

Instruction Hit

Tag

PA7100LC Die Photograph

(To Be Completed)
System Cost Reduction

- Integrated Memory and I/O Controller
- Direct Connection to DRAMs
- Single, Combined External Cache
- Uses Standard SRAMS, DRAMS, and SIMMs
- Requires Only 12 SRAM's Using x8 Technology
- With 12ns parts can run to 66MHz
- Low Power
- Mature VLSI Technology
- Reduced Cost Packaging
System Cost Reduction (Continued)

- Reduced Multiplier Array with No Degradation to Single Precision Flops
- Reduced Complexity for Long-Latency Flops
- 64 Entry Fully-Associative TLB
- Unified TLB with Lookaside Buffer
- Multimedia Improvements without Dedicated Hardware

Superscalar Instruction Bundling

**Instruction Classes**

<table>
<thead>
<tr>
<th>A: Integer ALU Operation</th>
<th>Rules</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shift/Merge Operation</td>
<td>Any 2 from separate classes or 2 integer ALU operation</td>
</tr>
<tr>
<td>Branch</td>
<td>L-L bundles for ldw or stw pairs to same doubleword address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>L: Int or FP Load/Store</th>
<th>Dynamic dependency checking</th>
</tr>
</thead>
<tbody>
<tr>
<td>E: Floating Point Operation</td>
<td></td>
</tr>
</tbody>
</table>
FP Latency and Issue Rates

<table>
<thead>
<tr>
<th></th>
<th>Single Precision</th>
<th>Double Precision</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add / Sub</td>
<td>2 / 1</td>
<td>2 / 1</td>
</tr>
<tr>
<td>Multiply</td>
<td>2 / 1</td>
<td>3 / 2</td>
</tr>
<tr>
<td>MPYADD / MPYSUB</td>
<td>2 / 1</td>
<td>3 / 2</td>
</tr>
<tr>
<td>Divide</td>
<td>8 / 8</td>
<td>15 / 15</td>
</tr>
<tr>
<td>Square Root</td>
<td>8 / 8</td>
<td>15 / 15</td>
</tr>
</tbody>
</table>

Virtual Memory Performance

- 8 Block TLB Entries, Each Map 512K - 64MBytes
- Hardware TLB-Miss Handler
- "Fast" TLB Insert Instructions
- GR Shadow Registers
Cache Performance

- External Cache Runs at Processor Frequency
- Pipelined Stores
- Address Hashing
- Cache Miss Optimizations
  - Instruction Streaming
  - Stall-on-Use
  - Hit-Under-Miss
  - Store-Under-Miss
  - Miss-Under-Miss
- Cache Hints
- Aggressive Instruction Prefetching

Instruction Prefetching
Memory and I/O Performance

- Dedicated 64-bit Memory Bus + 8 ECC Bits
- Tightly Coupled to CPU
  - Early Address Issue
  - Critical Doubleword First
- Uses DRAM Fast Page Mode
- Supports Extended Data Out Mode DRAMs
- Dedicated 32-bit I/O connection
  - DMA Concurrent with Cache Misses
- 50MB/sec Sustained CPU-Controlled Memory to I/O Transfer

Scalability

- Wide Range of Processor Frequency
- 48 Bit Virtual Addressing
- 8K to 2MBytes of External Cache
- 4M to 2GBytes of Main Memory
- Programmable DRAM latency and timing
- Programmable I/O Bus Frequency
Low Power Design

- Limited Use of Dynamic Circuits
- Elimination of PLA's
- Automatic Power-Up States
  - TLB
  - FP Megacells
  - Register Files
- Gating of Non-Overlapping Clock Nets

Design for Testability

- IEEE 1149.1 (JTAG) Compliant
- Parallel and Serial Block Tests
- Extensive Scannability
- Single-Step Capability
- IDDQ Static Current Testing
Summary

- Optimized For Low Cost Systems
- Performance Was Not Sacrificed
- Highly Configurable
- New Features
- Low Power
- Low Manufacturing Costs