The VelociTI™ Architecture of the TMS320C6xxx

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Agenda

◆ Motivation for Quantum Leap in DSP Performance
◆ The VelociTI™ Advanced VLIW Architecture
◆ VelociTI™ Pushes New Levels of DSP Performance
◆ Advanced Development Tools
◆ State-of-the-Art Process Technology
Motivation For Quantum Leap in Programmable DSP Performance

◆ Emerging demands for **mainstream applications** of *massively parallel, uniform DSP processing* in wireless or wireline communications

◆ Economic and engineering necessity to **reduce** system size and power consumption

◆ Rapid improvements in DSP algorithms, quickly evolving standards and shorter time-to-market

⇒ **VelociTI™** Advanced VLIW architecture opens up **unlimited possibilities** for *high-performance multi-channel, multi-function applications* by delivering **10x performance** over existing Digital Signal Processors
The VelociTI™ Advanced VLIW Architecture

TMS320C6x

C6x CPU Core

Program Fetch
Instruction Dispatch
Instruction Decode

Control Registers
Control Logic
Test
Emulation

Data Path 1
A Register File
L1 S1 M1 D1

Data Path 2
B Register File
D2 M2 S2 L2

TMS320C6x is not an evolution.
...not a revolution. 'C6x will fundamentally redefine digital signal processing solutions.

REDEFINES
VelociTI™ Advanced VLIW Architecture

Why VLIW?

◆ VLIW lends well to DSP algorithms and offers possibilities for very high performance
◆ VelociTI™ capitalizes on VLIW strengths while addressing its shortcomings with:
  ■ high silicon densities to improve speed paths through functional units
  ■ architectural innovations: flexible addressing modes, intelligent memory and peripheral support, flexible instruction packing and critical-path pipelining schemes
  ■ compiler-friendly: orthogonal, deterministic, 100% conditional RISC-like instruction set
  ■ advanced compiler and optimization technologies
NOTE: Control Register File, Pipeline, Interrupt Processing, Power Management and Emulation & Test Logic Blocks Are Not Shown.
VelociTI™ Advanced VLIW Architecture
First Offering: TMS320c6201

- 1,600 MIPS @ 200-MHz
- 5 ns internal cycle time
- Up to eight 32-bit instructions per cycle
- 3.3V I/O, 2.5V Internal
- 0.25 micron, 5-layer metal
- One Megabit On-Chip RAM
- SRAM, SB-SRAM, SDRAM Interface
- Four-Channel DMA
- Two MultiChannel T1/E1 Serial Ports
- 16-bit DMA Host Port
- 352-pin BGA
VelociTI™ Pushes
New Levels of DSP Performance
## VelociTI™ - New Levels of DSP Performance

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>‘C6x @ 200MHz</th>
<th>Typical DSP @ 60 MHz</th>
<th>‘C6x vs. Typical Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT (256-point)</td>
<td>14.0 us</td>
<td>199 us</td>
<td>14:1</td>
</tr>
<tr>
<td>DCT (8x8)</td>
<td>1.14 us</td>
<td>15.3 us</td>
<td>13.4:1</td>
</tr>
<tr>
<td>Viterbi – IS54 (89 terms)</td>
<td>29.5 us</td>
<td>315 us</td>
<td>10.7:1</td>
</tr>
<tr>
<td>LMS Filter (24 tap)</td>
<td>0.21 us</td>
<td>1.9 us</td>
<td>9:1</td>
</tr>
<tr>
<td>IIR Filter (8-biquads)</td>
<td>0.15 us</td>
<td>1.3 us</td>
<td>8.9:1</td>
</tr>
<tr>
<td>FIR Filter (24-tap, 64 data points)</td>
<td>3.9 us</td>
<td>31 us</td>
<td>8:1</td>
</tr>
</tbody>
</table>

New generation of tools use
- *advanced scheduling strategies* to achieve up to eight instruction in parallel every cycle
- *software pipelining techniques* to generate code that can execute multiple iterations of loops in parallel.
VelociTI™ - New Levels of DSP Performance
‘C6201 Multi-channel Application - Data Flow

ADPCM OUTPUT BUFFER

ADPCM INPUT BUFFER

MULTI-CHANNEL Vocoder

MULTI-CHANNEL LMS ECHO CANCELLER

DELAY BUFFER

COEFFICIENT LOOKUP TABLE

PCM INPUT BUFFER

PCM OUTPUT BUFFER

DATA BUFFER

EXPAND

DMA TO SERIAL PORT w/ COMPANDER

DMA TO SERIAL PORT w/ COMPANDER

Y[0]Y[1]
VelociTI™ - New Levels of DSP Performance

‘C6201 Multi-channel Application - Performance

• VLIW Signal Processing performance brings up to 40 channels of vocoders (ADPCM and Line Echo Cancellation) or 80 channels of ADPCM on a single-chip programmable DSP!

32K-bit ADPCM Implementation Statistics:

Program Memory: 8328 bytes (G.721 vocoder and LEC)
Data Memory: 39 KB total
(256-tap+256-coeff) * 32 channels * 2 bytes/word = 32KB for LEC
Cycles:
  Real time processing between samples provides 25K cycles/125 us.
Cycles for vocoder: 9.5K cycles per sample of 32 channels
Cycles for LEC: 10.5K cycles per sample of 32 channels
Total: 20Kcps \( \rightarrow \) \(<80\%\) of 200MHz ‘C6201
TI has shifted the DSP development paradigm from a hardware to software focus by supporting the programmable, high-performance 'C6x DSP with ultra-efficient, new-generation optimization tools.
Advanced Development Tools

Code Generation Flow

- Automated code generation handles scheduling complexities of traditional VLIW
- Tool suite support optimizing through an iterative programming process:
  - Use C Compiler to optimize and S/W pipeline
  - Use Assembly Optimizer to automatically schedule and optimize serial assembly code
  - Debug code through intuitive Windows-based source code (C and Assembly) debugger
- Optionally hand optimize only most critical functions
Cycle Counts for Unmodified C Benchmark Results

Cumulative Cycles of 8 Typical DSP Benchmarks (Data Courtesy EDN)

- TI C30: 22000
- Analog Devices SHARC: 26427
- TI C6x: 11988
- TI C54x: 41269
- Motorola 56300 (Tasking): 94163
- Motorola 56002 (Tasking): 188666
- Hitachi SH-DSP (Green Hills): 81982
- DSP Group OakDSP Core: 68621
Advanced Development Tools

Debug Tools Flow

• Software Only
• Win 95/NT

• Contains DSP
• PCI Card
• Avail 1Q98

• ISA card
• No DSP
• PC/Target
• JTAG cable

- Debug
- HEX6x
- ROM Prog.
- Target Board
- SIM6x
- EVM 6x
- EMU6x

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State-of-the-Art Process Technology

◆ C6201 will be manufactured with Timeline™ 0.18 micron process 1H98
◆ Higher speed version (250+ MHz) and derivatives to be expected in near future
◆ Higher levels of integration and peripheral mix using ASIC-flow are forthcoming
Summary

‘C6x VelociTI™ Advanced VLIW enables:

• Delivering 10x performance of any DSP on the market today.
• Shifting development paradigm from a hardware focus to a software focus.
• Establishing VelociTI Advanced VLIW as the architecture of choice for high-performance, low-cost DSP solutions.
• Reducing development time by half with new-generation tools designed for greatest ease of use and maximum optimization.
• Reducing system cost by half for multi-channel/multi-function applications.
• Opening the future to endless possibilities in real-time voice and data communications.