A Multi-threaded 64 Bit PowerPC Commercial RISC Processor

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Goals

- Very High Performance on Commercial* Benchmarks
- Scalability up to 24-Way Processors
- Multi-threading Operation up to Virtual 48-Way
- High L2 and Memory Bandwidth
- Low Latency Design
- Optimized Power, Area and Performance

* Commercial = TPC, SAP, SpecWeb and Lotus Notes

Outline

1. Commercial Overview
2. CPI Breakdown
3. L2 Miss
4. Processor Overview
5. Pipeline
6. MT Structures
7. MT GPR Cell
8. Peak Performance on Memcpy
9. Architecture for MT control registers
10. MPs Configuration
11. Performance Improvements with MPs
12. Industry Standard Benchmarks
13. Summary
14. Chip Plot
Commercial Server Code

**Typical String:**
1) LD; Fetch Record
2) CMP; Match Key
3) BC; Branch to Handler

**Characteristics**
Seldom Loops, as in Matrix Algebra
Large Working Set, frequent Read-Write sharing
Branch Prediction Difficult

Characteristics of Commercial Server Workloads

**Natural Task Level Parallelism**
Large Number of Users
Throughput is Primary Performance Measurement

**Significant Cache and Memory Component to CPI**
Trends in Memory Latency are Increasing
Commercial CPI Breakdown for Uniprocessor

Multi-threading Examples

No Multi-threading

Switch Threads on L2 Miss
### Processor Migration

<table>
<thead>
<tr>
<th></th>
<th>Northstar</th>
<th>Pulsar</th>
</tr>
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<tbody>
<tr>
<td>Frequency</td>
<td>350 MHz</td>
<td>450 MHz</td>
</tr>
<tr>
<td>MPs</td>
<td>12 Way</td>
<td>24 Way</td>
</tr>
<tr>
<td>Cache Size</td>
<td>128 KB</td>
<td>128 KB</td>
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<tr>
<td>L2 Peak BW</td>
<td>8.4 GB/s</td>
<td>14.4 GB/s</td>
</tr>
<tr>
<td>Mem Peak BW</td>
<td>1.9 GB/s</td>
<td>2.4 GB/s</td>
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<tr>
<td>Mem Bus Ratio</td>
<td>3:1</td>
<td>3:1</td>
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<td>Max Memory</td>
<td>40 GB</td>
<td>96 GB</td>
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<tr>
<td>Chip Size</td>
<td>162 sqmm</td>
<td>139 sqmm</td>
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<tr>
<td>Power</td>
<td>34W</td>
<td>22W</td>
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<td>7S, 1.8v</td>
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<td>Metallurgy</td>
<td>5-Al Bulk</td>
<td>6-Cu Bulk</td>
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</tbody>
</table>

### Processor Overview

![Processor Diagram](image-url)
Multi-Threaded Structures

MT Structures
- GPR, FPR and SPRs
- Queue Expansion for Extra Traffic

Non MT Structures
- IC, DC, TLB, FUs and MMU
"Memcpy" Diagram

Source or Destination Miss

non-MT Execution

thread 0:

thread 1:

MT Execution

Pulsar Performance Improvement for Memcpy applying MT
Architected MT Control Registers

- TSC<0:31> Thread Switch Control
  - Controls events for thread switching
  - L1 misses, L2 misses, TLB misses and etc.
- Priority Control Instructions
  - NOPs that set thread priority to lo, med, hi
  - NOPs are backward compatible
- TST<22:31> Thread Switch Time-out
  - Limits cycles that one thread is active
  - Prevents "infinite loop" task domination
- Forward Process Guarantee
  - Limits number of thread swaps from an instruction
  - Prevents threads from thrashing

Pulsar MP 24-Way System
Pulsar Performance Improvement
MT versus MPs

Top SPECweb Performance

Data as of: 13 July 99
Top TPC-C Clustered Systems

- IBM RS6000
- Compaq Alpha
- Sun Enterprise 6000

- 8nodex12w
- 8nodex12w
- 2nodex22w

- $122.44/tpmC
- $139.49/tpmC
- $134.46/tpmC

* Data as of 07/13/99 from:
  http://www.ideasinternational.com/benchmark/bench.html

Follow On Direction

- More MPs
- NUMA Options
- Bigger L2
- SMI interface
- Premier Technology "SOI"
- Low E Wire Technology
- Frequency Growth
- Constant Power Curve