MAP1000A: A 5W, 230MHz VLIW Mediaprocessor

Hot Chips ’99

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MAP1000A

- VLIW CPU + system-on-a-chip peripherals
- Based on MAP Architecture
  - Developed Jointly by Equator and Hitachi
  - Based on Multiflow Architecture and Compiler
- Second Device in MAP Family
  - 0.18u, 230MHz, 5W
Goals

• Transform Digital Media and Digital Imaging Platforms
  – Eliminate hardwired imaging engines
  – Merge high performance imaging into mainstream microprocessor
  – Bring “DSP revolution” to video rate products
    • need 80x+ vs. conventional DSP
  – System-on-a-chip for DTV back end
Existing Infrastructure: Fixed Function
The Mediaprocessor Platform

OpenCable™ STB / 3D Game Console
DVD Player / DVD Recorder
Web TV / Digital TV / HDTV Encoder
ADSL Concentrator / Cable Modem
Video Conference System / MFP Printer

MPEG2 Video Encoder
MPEG2 Video Decoder
AC-3 Audio Decoder
H.323
MPEG 4
IP Voice
V.34 Modem

Scheduler
Resource Manager
Communication Manager

Real-Time Microkernel

MediaProcessor

Interconnect
DRAM
Media Buffer
Frame Buffer

IP, Transport, NTSC In

Mother Board
Key Design Drivers

- **US ATSC HDTV decoding**
  - All formats input; resolution change for 1080i
  - Including transport, audio, OS, EPG, …

- **SDTV time shifting**
  - Concurrent MP@ML encoding and decoding

- **Advanced codec support**
  - Flexible datapaths; not just DCT engine

- **Many Developers, Multiple Operating Systems**
  - It’s a jungle out there
Chip Overview

- 18 - 23 GOPS 8-bit
- 8.7 GOPS 16-bit
- 1.8 GFLOPS 32-bit
Processor Core

• Registers:
  – 2 x 32 x 64 (or 2 x 64 x 32) GRs
  – 2 x 16 x 1 predicates
  – 2 x 2 x 128 PLs

• Functional Units
  – 2 32-bit iALUs, 2 64-bit iALUs
  – 2 32x2 FMAC
  – 2 32x2 FDIV/FSQRT
  – 2 64-bit partitioned integer/shift paths
  – 2 128-bit partitioned integer op / accum paths
Instruction Issue

- 4 operations packed per VLIW
- NOPs compressed out; “tag” field guides decode
- Fully Predicated 3-operand RISC architecture
- Over 1200 total opcodes
  - ~40 signal/image processing operations
  - data size
  - pre/post format / round
  - signed/unsigned
  - saturating/unsaturating
Issues and Opportunities

• Deep-Pipeline Organization for Voltage Reduction
  – Lbr=3, Lld=5, Lfmac=5, Limac=5, Liadd=1
  – Push Problems Back at Compiler

• Wide Parallel Computation
  – VLIW and MicroSIMD
  – Algorithm-Optimized Datapaths

• Image Computing Means High Data Movement
  – 4 x 64-bit ports, 16-deep nonblocking, 16K D$
  – No pure cache-based solutions suffice
  – Explicit data movement programming
Partitioned Inner Product Operations

- 8 16x16 Mpy-accumulate per cluster per cycle
- Multiply and Add can be selectively turned on
- Partitioned 8-bit, 16-bit, and 32-bit
Partitioned Distance Ops

\[ \text{result} = \sum_{i=0}^{15} |A(i) - B(i)| \]

\[ \text{result0} = \sum_{i=0}^{7} |A(i) - B(i)| \quad \text{result1} = \sum_{i=8}^{15} |A(i) - B(i)| \]
Tools Issues

• Chip-Level Simulators
  – Fast Core-Only
  – Fast Full-Chip
  – Full-chip Cycle-Accurate

• Compiler Issues
  – High ILP, Multiple Register Banks
  – Deep Pipelines, Exposed Resources, Wide Issue
  – Media Function and DS support
  – “99% of Machine Peak” -- NEVER revert to asm
From Media Opcodes to Media Datatypes

void pixadd(
  unsigned char *restrict input8,
  short *restrict input16,
  unsigned char *output,
  int pixCnt
)
{
  for (int k = 0; k < pixCnt; k++) {
    int pixOut = input8[k] +
                 input16[k];
    pixOut = pixOut < 0xff ?
             pixOut : 0xff;
    output[k] = pixOut > 0 ?
               pixOut : 00;
  }
}

void pixadd (  
  long *restrict input8,  
  long long *restrict  
                input16,  
  long *restrict output,  
  int pixCnt
)
{
  for (int k = 0; k <
       pixCnt / 4; k++) {
    output[k] =
                compress_ps16_pu8_sa(  
                             add_ps16_sa( expand_pu8(  
                                             input8[k] ),  
                                             input16[k] ) ) ;
  }
}

void pixadd(
  p32u8 *restrict input8,
  p64s16 *restrict input16,
  p32u8 *restrict output,
  int pixCnt
)
{
  for (int k = 0; k <
       pixCnt / 4; k++) {
    output[k] =
                (p64s16)input8[k]  
                +(sa) input16[k] ) ;
  }
}
Coprocessor and DS

3D Graphics

Video Scaler

16-bit RISC co-processor memory

I-ALU
IFG-ALU
I-AU
IFG-ALU

Data Cache

Register File

Instruction Cache

VLIW core

ITAG

PCI-A

PCI-B

HDL C
CRC

DataStreamer

Glueless SDRAM Controller

Display Refresh Controller

AC-Link

I²C

ITU-R BT.656 OUT
ITU-R BT.656 IN
FLASH ROM LF

I/P Switchable pin selector

ITU-R BT.656

Transport Channel Interface

I²C

IEC958

PLLs

32-bit 66MHz

32-bit 66MHz

24.576MHz

Analog RGB
Data Streamer

- PCI
- VLIW
- MC

Data Streamer:
- Request Engine
- Buff Cntlr
- 4K SRAM

- 64 buffers
- 64 FIFO pointers

64 Address Generation channels
Data Streamer

PCI

Data Streamer

VLIW

MC

Request Engine
Buff Cntlr
4K SRAM

1 of the 64 fifos
Data Streamer

- PCI
- MC
- VLIW
- Request Engine
- Buff Cntlr
- 4K SRAM
- FIFO

1 of the 64 address generators
Memory resident descriptor controls each transfer
this one transfers from memory to the fifo buffer
Linear sequential address generation for “width” bytes
Data Streamer

PCI

VLIW

MC

2D BLT like addressing (pitch, width, line count)
Another data streamer channel transfers from the fifo buffer to memory.
Data Streamer

Descriptors can be chained
Data Streamer

Can specify Cache Coherent Destinations
(used for idct cache prefetching)
SW Genlock Considered Harmful
Die Photo
Video Usage Scenarios

- MP@ML view
- MP@HL view
- Analog Timeshift
- Dual TV MP@ML
- 4 Stream Decode
- VideoConf 30fps CIF
- Streaming Video En...
- Analog View
- 3D Gaming

Legend:
- Encode
- Noise Reduction
- Transport Demux
- Audio Decode
- Video Decode
Mediaprocessor Summary

• Fixed-Function Platform:
  – Each Feature Adds Cost
  – Must Decide At Time Of Product Deployment
  – Delays in Development/ New services / New revenues

• Mediaprocessor
  – “DSP Revolution” Comes to Video/Media/Imaging
  – Appropriate Silicon Available NOW
  – Cost at parity in 2000, lower by 2001
  – Rapid Rollout New Features / Services
    • Internet-Ready Consumer Electronics