C-5 DCP Network Processor

System Scaling
CSIX Standard
Custom Interconnects

Networking Intelligence
Traffic Classification
Policy Enforcement
VPN & MPLS Services
Quality of Service
Switching / Routing
Interworking, ...

Physical Layer
(DS-1 through OC-48 rates)
T/E-Carrier, Ethernet, SONET,
FR, POS, ATM, DWDM, Fibre Channel

5 Gbps Aggregate Bandwidth
10 Gbps Aggregate Bandwidth
Terabits of Aggregate Bandwidth
C-5 DCP Functional Block Diagram

C-5 Digital Communications Processor

Table Lookup Unit

Fabric Processor

Queue Management Unit

Buffer Management Unit

Ring Bus

Payload Bus

Global Bus

Control Logic (Opt.)

External PROM (Opt.)

Serial Interface

PROM Interface

PCI Interface

16 Channels

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Channel Processors: Scale with Parallel and / or Pipelined Processing

- Single CP processes full duplex wire-speed data up to 155Mbps

- **CP Aggregation** scales bandwidth
  - CPs organized into parallel clusters (4 CPs per cluster)
  - Built-in sequencing scheme maintains simple programming

- **CP Cascading** scales processing
  - CPs linked for pipelined processing on single data stream
  - Internal data recirculation enables flexible CP assignment
Channel Processor: RISC Core plus dual parallel Serial Data Processors

- **Channel Processor RISC Core**
  - Harvard Architecture
  - Quad-ported IMEM (24K)
  - Quad-ported DMEM (48K)
  - Optimized instruction set for networking applications

- **Serial Data Processors**
  - Bit and byte-level micro-sequencers
  - Programmable field parsing / extraction / insertion / deletion
  - CRC validation & calculation
Serial Data Processors

- Configurable pin logic for connection to a wide variety of physical interface types
- On-chip functional integration
  - 10/100 Ethernet MACs
  - GbE MACs
  - OC-3/12 SONET framers
  - HDLC Controllers
  - ATM Cell Delineation
  - FibreChannel
- Adaptable to future and / or proprietary interfaces
**Channel Processor RISC Core**

- **Multi-context RISC architecture**
  - 4 independent register sets for fast context switching
  - 4 independent data scopes for multi-task performance
  - Extract, merge memory and queue status registers for header & data management
  - 64-bit event register for efficient polling
Table Lookup Unit: Specialized Co-Processor for Table Manipulation

- Implements complex L2/3/4+ lookups
  - hash, exact match, longest prefix match, etc.
- Supports multiple lookup algorithms simultaneously
- Internally pipelined
- Up to 133M lookups/sec (max)
- Tables implemented in 64 bit, 133MHz ZBT SRAM
  - Up to 64MB in four banks
Buffer Management Unit: Specialized Co-Processor for Buffer Manipulation

- Implements simple buffer tag scheme
  - Supports multicast buffer counters
- Up to 16 Gbps maximum bandwidth
- Up to single bank SDRAM (128MB)
- Built-in error-correction / detection
  - 139-bit interface, up to 125MHz (128 bits data, 9 bits ECC)
- Configures up to 30 different pools
  - Buffer sizes from 64 to 64K bytes
  - Up to 64K buffers per pool
Queue Management Unit: Specialized Co-Processor for Queue Manipulation

- Implements programmable queuing mechanisms
  - Automated multicast elaboration
- Built-in thresholds for multi-class buffer management
  - Up to 4 usage pools
  - Separate allowance & limit per pool
- Implements up to 512 queues
  - Flexible per processor allocation
  - Up to 16,384 descriptors
- Descriptors stored in 32-bit, ZBT SRAM (128K max) at 1/2 core clock frequency
Fabric Processor: Specialized Co-Processor for Fabric Connection

- Flexible support for many interfaces
  - Utopia 2 and Utopia 3
  - Glueless for some industry fabrics
  - Configurable for proprietary fabrics
- Programmable fabric parameters
- Flow and congestion control
- Segmentation and re-assembly
- >15M packets/cells per second
- Integrated scheduling up to 128 Q’s
- 3.2 Gbps full-duplex maximum
  - 100Mhz, 64bits (32bit Tx / 32bit Rx)

• Utopia 3
• Utopia 2
• IBM
• Power-X
• ...etc.

Motorola & C-Port Corporation Confidential
Executive Processor: Specialized Co-Processor for Auxiliary Management

- Auxiliary processor for internal chip management
  - Reset, initialization, configuration
  - External host communication
  - Statistics harvesting
  - Table maintenance, etc.
- Standard RISC instruction subset
- External interfaces
  - 32-bit, 33/66MHz PCI bus (Host)
  - Optional Serial PROM (Program)
  - 2-wire, configurable bi-directional serial bus (I2C-like or MDIO for LEDs, PHY control, etc.)
- Three optimized buses separate control / data:
  - Payload Bus: data movement
  - Ring Bus: controlled latency transfers
  - Global Bus: general inter-processor messaging
- Global bus provides flat memory space across all processor memories

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>Bus Width</th>
<th>Transfer Size</th>
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<tbody>
<tr>
<td>Payload Bus</td>
<td>~35 Gbps</td>
<td>128 bits</td>
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<tr>
<td>Ring Bus</td>
<td>~22 Gbps</td>
<td>64 bit</td>
</tr>
<tr>
<td>Global Bus</td>
<td>~4 Gbps</td>
<td>128 bits</td>
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Application Example: Channel Forwarding Operation
C-5 DCP Methodology

- Time-to-market driven
  - few in-house tools

- Industry standard tools:
  - logic synthesis
  - place and route
  - verification

- Mixture of semi- custom and custom
  - 16.4M semi- custom x-tors, 40M custom x-tors

- Semi- custom
  - control structures

- Custom design where highest benefit
  - SRAMs, CAMs, buses, pads, clocks, ECC, etc.
C-5 DCP Summary

- 200 Mhz
- 17 RISC Cores
- 32 Serial Data Processors
- 5 Co-Processors
- Integrated memory and multiple buses
- Approximately 56M Transistors
- 0.18 um CMOS process
- 1.8V VDD
- 838 pin BGA Package
- JTAG Compliant