A 12-bit 50Mpixel/s Analog Front End Processor for Digital Imaging Systems

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Bird’s Eye View of Digital Camera

- A complete system from sensor to storage
Digital Camera System
Bird’s Eye View of Digital Camera

- A complete system from sensor to storage
- 300Kpix  1Mpix  2Mpix  3Mpix
Digital Camera Requirements

DSC

DVC

High Definition TV

10Mpixel/s
Problem!

- A complete system from sensor to storage
- 300Kpix  1Mpix  2Mpix  3Mpix
- Slow speed !!!
- Short battery life !!!
Another Problem!? 

• A complete system from sensor to storage 
• 300Kpix  1Mpix  2Mpix  3Mpix
Serious D-Range Problem!

300Kpix  1.3Mpix
Problem’s!

- A complete system from sensor to storage
- 300Kpix  1Mpix  2Mpix  3Mpix
- Slow speed !!!
- Short battery life !!!
- Low dynamic range !!!
  - 10bits    12bits,
Performance Goal

- **Frame/s**: 0 10 20 30 40 50 60 70
- **Mpixel**
  - 7
  - 6
  - 5
  - 4
  - 3
  - 2
  - 1
  - 0
- **DSC**
- **DVC**
- **High Definition TV**

- **Performance Goal**:
  - 10bit ➔ 12bit
  - 10Mpixel/s ➔ 50Mpixel/s
More D-Range Problem!

Color Noise in gray area
Color Noise in half tone area

Problem of current AFE
No analog white balance

Color Noise due to different quantization error.
Spectrum Change

Image Sensor

Micro Lens
Color Filter
Photo Diode

Wave Length
Transparency

100%
B
G
R

100%
B
G
R

B
G
R

100%
B
G
R

2000/8/6
NuCORE Technology Inc.
NDX enables analog white balance

- Equalize Color D-Range before A/D
- Color spectrum vary caused by; filter, light source, scene, etc., need color by color compensation

3 CCD Camera → “Single CCD + NDX” Camera
Technical Challenges

* 12-bit accuracy along entire image chain
* Color by color gain control in Analog \( NDX^{tm} \)
* Very low power dissipation
* >50 Mpixel/s <20 nsec time budget!

13 patents pending
NC1250 - Analog Front End
NDX Circuit Techniques for Fast Gain Changes on the fly

• Switched-capacitor circuits for analog signal processing
• Multi switched-capacitor banks with shared opamps
• Crosstalk minimization
• Power/performance trade-off:
  - stage scaling
  - programmable bias level
NDX  
CDS/PGA Architecture

Multi switched-cap banks

10-Bit D/A Converter

vga(0)-vga(3)  vga(4)-vga(7)
Conceptual Scheme of a part of switched-cap. banks
12-bit 50 MS/s ADC

- Pipeline architecture
- Auto-calibration and digital correction
- DNL, INL < 1 LSB
- SNR >TBD dB
- THD < -TBD dB
- Internal reference generator and buffers
ADC Circuit Techniques for 12-bit 50 MS/s

- Switched-capacitor circuits for analog signal processing
- Dual switched-capacitor banks with shared opamps
- Crosstalk minimization
- Power/performance trade-off:
  - stage scaling
  - programmable bias level
ADC Architecture

Conversion Core (17 stages)

Reference Buffers

Calibration/Digital Correction

Dout

Vinp Vinn

Vrefp Vcom Vrefn

clk

bias

power control

12 (cal)

18 (data)

12

Dout<12:1>
ADC Architecture

Dual switched-cap banks


Chip Photomicrograph
Sample Image
Summary

• 12-bit 50 MS/s digital image acquisition system
• Up to 4 color specific gain setting (complementary color scheme compatible)
• Very low power design (120 mW~50mW)
• Overall system SNR > 60 dB

World Fastest AFE; 12-bit, color by color PGA enables High Definition DSC & DVC