Transmeta’s Crusoe:
Cool Chips for Mobile Computing

David R. Ditzel
Chief Executive Officer
Transmeta Corporation
Agenda

Transmeta’s Crusoe Technology

Crusoe Microprocessors

Introduction of a new Crusoe processor

Hardware support features for Dynamic Translation

A few Crusoe Systems
What are the big problems for designers of Mobile Computers that need to talk to the Internet?

Heat
High performance processors take 10 to 20 watts
Makes battery life unacceptably short.

Compatibility with the Internet
Need x86 compatibility to run
PC Software
Web based software - such as macromedia flash
Browser plug-ins (plug-ins are tiny x86 programs)

Performance
Need PC desktop levels of performance for good experience

Transmeta’s Crusoe Chip can solve these problems
Crusoe is a Family of Mobile Internet Processors

Low Power - for long battery life -- no fans

Compatible - with all x86 PC software

High Performance - for Internet applications
  • Streaming video (eg MPEG-4)
  • Macromedia Flash
How is Crusoe able to achieve these goals?

**Crusoe**

is the first microprocessor whose instruction set is implemented entirely with Software
Transmeta’s Vision: A Software Based Microprocessor

- New Idea: software could be an integral part of a microprocessor
- A combined hardware/software solution could have many benefits
  - Simpler hardware chips
  - Easier to design and debug chips
  - Smaller design teams with shorter design times
  - No worry about backward compatibility in hardware
  - Less costly to manufacture smaller chips
  - Simpler chips would run cooler

Plus software could LEARN as it ran – the first SMART processor
Crusoe Technology and Benefits

Crusoe is the sum of

- Code Morphing Software
  - Dynamic x86 to VLIW translator
  - Software optimized execution
  - Learns and improves with time

- VLIW Processor
  - 128-bit Very Long Instruction Word
  - Simple and fast Engine
  - Significant reduction in transistors

\[
\begin{align*}
\frac{3}{4} &+ \frac{1}{4} = \frac{4}{4}
\end{align*}
\]

Low Power

x86 Compatibility

PC Performance
### Conventional HW vs Crusoe HW+SW

<table>
<thead>
<tr>
<th>Conventional x86 Silicon Hardware</th>
<th>VLIW Silicon Hardware</th>
<th>Code Morphing Software</th>
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</thead>
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<tr>
<td>variable length instruction decode</td>
<td>simple decode</td>
<td>x86 decoding</td>
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<tr>
<td>superscalar grouping logic</td>
<td>instruction grouping</td>
<td>instruction scheduling</td>
</tr>
<tr>
<td>superscalar issue logic</td>
<td></td>
<td>bypass scheduling</td>
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<tr>
<td>bypass logic</td>
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<td>register renaming</td>
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<tr>
<td>register renaming</td>
<td></td>
<td>address mode synthesis</td>
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<tr>
<td>complex addressing modes</td>
<td>in-order execution</td>
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<tr>
<td>out-of-order execution</td>
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<td>speculative execution</td>
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<td>arithmetic functions</td>
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<td>register files</td>
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<td>software libraries</td>
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<tr>
<td>microcode ROM</td>
<td>caches</td>
<td></td>
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<tr>
<td>caches</td>
<td></td>
<td>fp stack</td>
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<tr>
<td>fp stack logic</td>
<td></td>
<td>code optimization</td>
</tr>
</tbody>
</table>
The First Two Crusoe Processors

- TM5400
  - 700 MHz
  - 400 KBytes of cache
  - 1 watt
  - x86 compatible

- TM3200
  - 400 MHz
  - 108 Kbytes of cache
  - 1 watt
  - x86 compatible

Lightweight Notebook Computers
Microsoft Windows
Mobile Internet Appliances
Mobile Linux
TM5600: A New Crusoe Processor

- New TM5600 Crusoe Processor
- Same package pinout as TM5400
- 700 MHz operation with LongRun
- 656 KBytes of on-chip cache
- L2 increased to 512K bytes
- Performance increases by ~20% at same MHz
- Power reduced by ~10%

Lightweight Notebook Computers
Microsoft Windows
### TM3200 for Mobile Internet Devices

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>333-400 MHz</td>
</tr>
<tr>
<td>L1 Cache</td>
<td>96KB</td>
</tr>
<tr>
<td>L2 Cache</td>
<td></td>
</tr>
<tr>
<td>Main Memory</td>
<td>PC133 SDRAM</td>
</tr>
<tr>
<td>Upgrade Memory</td>
<td>Integrated</td>
</tr>
<tr>
<td>North Bridge</td>
<td>474 BGA</td>
</tr>
<tr>
<td>Die Size</td>
<td>77 mm²</td>
</tr>
<tr>
<td>Sample Production</td>
<td>Now</td>
</tr>
<tr>
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TM5400 for 2-4 Lb. Ultra-Light PCs

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<tr>
<th>Specification</th>
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</tr>
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<tbody>
<tr>
<td>Frequency Range</td>
<td>500 – 700 MHz</td>
</tr>
<tr>
<td>L1 Cache</td>
<td>128K</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>256K</td>
</tr>
<tr>
<td>Main Memory</td>
<td>DDR or SDRAM</td>
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<tr>
<td>Upgrade Memory</td>
<td>SDRAM</td>
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<tr>
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<tr>
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<tr>
<td>Process Technology</td>
<td>.18u</td>
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<tr>
<td>Die Size</td>
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<tr>
<td>Sample</td>
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# TM5600 for 2-4 Lb. Full Featured Notebooks

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**TM5600**
Crusoe VLIW Processor Architecture

Free from x86 Legacy

- 128 bit VLIW processor
  - Simple 6 Stage Pipeline
  - Fetch0
  - Fetch1
  - Decode
  - Register Read
  - Execute
  - Register Writeback

Code Morphing HW support

Integrated North Bridge
- PC133 SDR DRAM Controller
- DDR DRAM Controller
- PCI Bus Interface
Crusoe VLIW Processor Instruction Formats

C = 1 bit Commit instruction
sw = 2 bits for software use
Memory = Load or Store
ALU operations are 3 address register to register ops with 64 general registers
Compute = ALU1, Floating Point or Multimedia op

Transmeta Hot Chips Presentation - August 2000
Crusoe’s Hardware Support for Dynamic Instruction Translation

or

How to make life easier for software
Traditional Code Generation Headaches

Life would be so much easier if it weren’t for:
• Not enough registers
• Branches (basic blocks too short)
• Pointers
• Interrupts
• Faults
• Need to preserve original program order
• Self modifying code

Crusoe’s hardware has support for all of the above
Basic Support

Lots of Registers
- 64 Integer Registers
- 32 Floating Point Registers

Lots of Cache
- 64 KB Level 1 Instruction Cache
- 64 KB Level 1 Data Cache
- 512 KB Level 2 combined I+D Cache
- 8 KB software managed local data memory
- 8 KB software managed local instruction memory

Simple pipeline
- 1 128-bit VLIW instruction (molecule) per clock
- Up to 4 atoms (RISC like op) per molecule
- So Software can tell the cost of an instruction!
Crusoe: Forgiveness and Time Travel

On typical processors, code generation must be very conservative
- Must generate code that is “correct” in all cases
- Very rare circumstances ruin opportunities for optimization
  - e.g. memory aliases of two pointers
  - e.g. unexpected faults
- Less data in registers, more loads and stores
- Less speculation
- Result is less optimal code

Crusoe encourages aggressive optimization and speculation
- If rare circumstances happen:
  - Give forgiveness
  - Travel back in time to before the exceptional event
  - Redo the event with more conservative code generation
Advanced Hardware Support

- Shadowed Register Files
- Gated Store Buffer
- Commit / rollback instructions
- Alias hardware
- Compare and Trap instructions
- Select instructions
Shadowed Register Files

- Two copies of registers: working and shadow.
  - 64 Integer registers with 48 shadows
  - 32 Floating point registers with 16 shadows
- Normal atoms read/write working registers
- commit and rollback atoms copy working ↔ shadow
Gated Store Buffer

- Similar to traditional write buffer, except...
- \textit{GATE} delays stores until next commit instruction or Rollback instruction can undo stores

```
Id/st unit \textbf{GATE} \rightarrow to memory
```
Load / Store Reordering

- Reordering register-register ALU ops is easy
- Reordering loads and stores: harder
- Need knowledge about memory addresses

The above transformation FAILS if pointers x equals y, so this optimization is rarely used
Crusoe Alias Hardware

- Crusoe has unique Alias detection hardware
- Software uses special ld/st atoms when reordering
- Trap if memory regions overlap
- Ex: load protects memory, store checks
- Software can take corrective action, but rare

Correctness can be guaranteed, and easy to use
Crusoe Alias Hardware (e.g. #2)

Alias hardware can allow software to safely \textit{eliminate} memory operations

\begin{align*}
\text{ld} & \ %r30, [\%x] \quad & \text{ldp} & \ %r30, [\%x] \\
\ldots & \text{ld} & \ %r31, [\%x] \quad & \text{st} & \ %r30 \\
\text{st} & \ %r30, [\%y] \quad & \text{stam} & \ %r31, [\%y] \\
\text{use} & \ %r30 \\
\text{use} & \ %r31
\end{align*}

Correctness can be guaranteed, and easy to use
Multi-block Example

**x86 (IA-32) Instruction Mix**

1. movl %ecx,$0x3
2. jmp lbl1

**lbl1:**

3. movl %edx,0x2fc(%ebp)
4. movl %eax,0x304(%ebp)
5. movl %esi,$0x0
6. cmpl %edx,%eax
7. movl 0x40(%esp,1),$0x0
8. jle skip1
9. movl %esi,0x308(%ebp)
10. movl %edi,0x300(%ebp)
11. movl 0x7c(%esp,1),%eax
12. cmpl %esi,%edi
13. jle skip2
14. xorl %eax,%eax
15. movl 0x6c(%esp,1),%esi
16. cmpl %edx,%eax
17. movl %eax,$0x1
18. xorl %eax,%eax
19. movl %esi,0x308(%ebp)
20. jnl exit1

**skip1:**

21. movl 0x6c(%esp,1),%esi
22. cmpl %edx,%eax
23. movl %eax,$0x1
24. xorl %eax,%eax

**skip2:**

25. movl %esi,0x308(%ebp)
26. movl %edi,0x300(%ebp)
27. movl 0x7c(%esp,1),%eax
28. cmpl %esi,%edi
29. movl %eax,$0x1
30. jnl exit1

**exit2:**

31. br <exit1>

**“Morphed” (128-bit) VLIW Instructions**

1. addi %r39,%ebp,0x2fc;commit
2. addi %r38,%ebp,0x304
3. ld %edx,[%r39]; add %r27,%r38,4; add %r26,%r38,-4
4. ld %r31,[%r38]; add %r35,0,1; add %r36,%esp,0x40
5. ldp %esi,[%r27]; add %r33,%esp,0x6c; sub.c %null,%edx,%r31
6. ldp %edi,[%r26]; sel #le %r32,0,%r35;
7. stam 0,[%r36]; sel #l %r24,%r35,0; add %r25,%esp,0x7c
8. stam %r32,[%r33];add %ecx,0,3; sub.c %null,%esi,%edi
9. st %r24,[%r25]; or %eax,0,0; brcc #lt,<exit2>
10. br <exit1>
Crusoe can be used in a Range of Mobile Computers

Crusoe in Mobile Internet Computers

Mobile Client  Web tablet  Thin+light Mobile PC  Full featured Mobile PC
Crusoe Offers Advantages for Mobile Internet Computing

- Battery life
- Size and weight
- No noisy fans
- Full PC software compatibility
- LongRun power management

Low power is the key.