20Gb/s 0.13um CMOS Serial Link

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Outline

• Motivation

• Background
  ‣ Static phase offset
  ‣ Random/power supply induced jitter

• Proposed 20Gb/s transceiver
  ‣ New Architecture
  ‣ Circuit Blocks
  ‣ Receiver Design
  ‣ Preliminary Results

• Conclusion
I/O Bandwidth is Limiting Factor

- Predicted Off-Chip Bandwidth growing slower than On-Chip

- Higher bit rate I/O’s needed to close this gap

Predicted Maximum On-Chip vs. Maximum Off-Chip Bandwidth

- Total I/O BW calculated from total I/O pins * I/O bandwidth/pin.
- Total on-chip BW calculated from on-chip clock frequency * # wires/chip
20Gb/s 0.13um CMOS Transceiver Goals

• Design I/O architecture that minimizes timing uncertainty
  ‣ Systematic/static phase offset
  ‣ Random/power supply induced jitter

• Not addressing channel equalization

• Reasonable power dissipation(200mW/link)

• Small area footprint(500um x 500um) for high integration on single chip
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Static Phase Offset—Ideal Transceiver

Timing Margin = 12ps
Static Phase Offset—Reality

10ps static phase offset

Actual Transmitter Output

Timing Margin=7ps 42% reduction

Actual Receiver Input
Power Supply Induced Jitter

Supply Noise

Transmitter

+ +
- -
Outa Outb

Receiver

- -
+ +
Ina Inb

VDD

Sampling Clock

10ps pk-pk Supply Induced Jitter

10ps pk-pk Supply Induced Jitter

25ps 15ps 25ps 15ps

Actual Transmitter Output

25ps 15ps 25ps 15ps

Actual Receiver Output

Timing Margin=2ps

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20Gb/s Transmitter Design Spaces

1:1 Multiplexer at f

- 20Gb/s
- 1 phase @ 20GHz

2:1 Multiplexer at f/2

- 20Gb/s
- 10Gb/s
- 2 phases @ 10GHz

N:1 Multiplexer at f/N

- 20Gb/s
- 5Gb/s
- 5Gb/s
- 5Gb/s
- 4 phases @ 5 GHz

Choose this Architecture

Low jitter / power supply induced jitter

Low static phase offset

Difficult to design

Large area

High jitter / Larger power supply sensitivity

Large static phase offset

Easy to design

Small Area

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New Architecture

```
8 data signals @ 2.5Gb/s

4:1 Mux

D0
D1
D2
D3

“Dirty” Multi-Phase Clocks

10Gb/s

4:1 Mux

D0
D1
D2
D3

“Dirty” Multi-Phase Clocks

10GHz Latch

10Gb/s

10GHz Latch

10Gb/s

2:1 Output Mux

20Gb/s

“Clean” 20Gb/s

Timing uncertainty based solely on last stages, clocked by 10GHz clock

“Clean” 2-Phase 10GHz CLK

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New Architecture Reduces Jitter/Phase Offset

Two 10Gb/s Data Streams

2-phase 10Ghz Clock

20Gb/s Output

Can tolerate jitter/static phase offset here
20Gb/s Transmitter

Low Static Phase Offset
Low Supply Induced Jitter

No post-PLL Buffers
20Gb/s Output Stage

- 10GHz clock sources directly from LC oscillator tank
- No post-PLL buffer jitter
- Low static phase offset
- Simulated data-dependent jitter is minimal

Calibration Scheme

- Send DC balanced “1010” pattern
- Sample 20Gb/s output with uncorrelated clock
- Adjust variable capacitance based upon output sampling histogram
10GHz Analog Latch

- Full pass gates provide symmetric clock injection
- Gain loss of $\frac{1}{2}$ from 10Gb/s input to output
4:1 10Gb/s Mux Design

8 Data Streams @ 2.5Gb/s

4:1 Mux

Data0_bot
Data1_bot
Data2_bot
Data3_bot

D0-top
D1-top
D2-top
D3-top

250 Ohm On-Chip Resistor

Data / Clock Gating

D0-bot
D1-bot
D2-bot
D3-bot
10GHz Clock Alignment Problem

- How do you ensure 10Gb/s data is in phase with 10Ghz clock?

Two 10Gb/s Data Streams

Mid0a

Mid0b

Mid1a

Mid1b

2-Phase 10GHz Clock

20Gb/s Output

Static Phase Offset/Jitter Passed to Output
Align zero crossings of 10GHz clock and 8 multi-phases of 2.5GHz Clock
Phase Interpolator

- Tri-state inverters provide coarse interpolation
- Digitally switch capacitors provide fine control
- Maximum phase step = 7.3ps
**10GHz LC Oscillator**

- Use passive L,C elements for frequency synthesis
  - 10x less jitter/power supply sensitivity than ring oscillator VCO’s
  - Significantly less static phase offset
  - Higher frequency of oscillation

- Disadvantage--area is significantly larger than conventional techniques
  - Area disadvantage mitigated by higher frequency--inductor size reduces by factor of 4 for 2x increase in frequency
  - A 130um x 130um 1nH inductor deemed reasonable area / per IO

- Tuning range given by inversion mode PMOS capacitors

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Regulated Supply provides additional power supply rejection

< 3ps pk-pk jitter--2000 cycles, with 20mV wideband Vdd noise
Receiver Design

- Clock recovery done at reset time
  - Sampling clock swept across entire bit period at reset time
  - Bit error is measured for sampling instances, and optimum sampling time chosen at startup
  - Periodic retraining of receiver to compensate for slowly varying timing drift
Simulated Results

Transmitter Layout Simulated 20Gb/s Output, with Clean Supply

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>20Gb/s</td>
</tr>
<tr>
<td>Process</td>
<td>1.2V, 0.13um Generic CMOS</td>
</tr>
<tr>
<td>Power</td>
<td>200mW(transmitter &amp; receiver) (PLL=20mW)</td>
</tr>
<tr>
<td>Estimated Area</td>
<td>500um x 500um</td>
</tr>
<tr>
<td>Pk-Pk Jitter</td>
<td>&lt; 10ps, with 20mV Vdd Noise</td>
</tr>
<tr>
<td>Output Swing</td>
<td>100mV</td>
</tr>
<tr>
<td>Input Receiver Sensitivity</td>
<td>40mV</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>10ps (10%)</td>
</tr>
</tbody>
</table>
Conclusion

• A 20Gb/s CMOS I/O Link has been designed

• Low Power, Low Area enable high integration of these 20Gb/s I/O pads on a single chip
Acknowledgements

- Velio Communications—Ramesh Senthinathan, Mark Kellam, John Poulton
- Jaeha Kim, Mark Horowitz, Niranjan Talwalkar for discussion
## BW Numbers

<table>
<thead>
<tr>
<th></th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
</tr>
</thead>
<tbody>
<tr>
<td># of pins</td>
<td>1600</td>
<td>1792</td>
<td>2007</td>
<td>2248</td>
<td>2518</td>
<td>2820</td>
<td>3158</td>
</tr>
<tr>
<td>I/O bw/pin</td>
<td>1.92E+09</td>
<td>2.77E+09</td>
<td>3.20E+09</td>
<td>3.50E+09</td>
<td>3.70E+09</td>
<td>4.00E+09</td>
<td>4.07E+09</td>
</tr>
<tr>
<td>total I/O bw</td>
<td>1.54E+12</td>
<td>2.77E+12</td>
<td>3.21E+12</td>
<td>3.94E+12</td>
<td>4.66E+12</td>
<td>5.64E+12</td>
<td>6.43E+12</td>
</tr>
<tr>
<td>on-chip bw/wire</td>
<td>1.20E+09</td>
<td>1.40E+09</td>
<td>1.60E+09</td>
<td>1.72E+09</td>
<td>1.86E+09</td>
<td>2.00E+09</td>
<td>2.12E+09</td>
</tr>
<tr>
<td>chip size</td>
<td>1.76E-02</td>
<td>1.76E-02</td>
<td>1.76E-02</td>
<td>1.80E-02</td>
<td>1.84E-02</td>
<td>1.89E-02</td>
<td>1.93E-02</td>
</tr>
<tr>
<td>minimum wiring width (16l)</td>
<td>1.44E-06</td>
<td>1.44E-06</td>
<td>1.04E-06</td>
<td>1.04E-06</td>
<td>1.04E-06</td>
<td>7.20E-07</td>
<td>7.20E-07</td>
</tr>
<tr>
<td># of wires</td>
<td>1.22E+04</td>
<td>1.22E+04</td>
<td>1.69E+04</td>
<td>1.73E+04</td>
<td>1.77E+04</td>
<td>2.63E+04</td>
<td>2.68E+04</td>
</tr>
<tr>
<td>Total on-chip BW</td>
<td>1.46E+13</td>
<td>1.71E+13</td>
<td>2.72E+13</td>
<td>2.98E+13</td>
<td>3.30E+13</td>
<td>5.30E+13</td>
<td>5.68E+13</td>
</tr>
</tbody>
</table>