JIO: High Performance I/O & Graphics For UltraSPARC IIIi-based Systems

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JIO Design Goals

• Integrate high-bandwidth, low latency interfaces on single chip:
  • Industry standard PCI I/O and Sun UPA 64S Graphics
  • Reduce system complexity/cost
• Interface with JBUS system bus
• Support 1 - 4 way UltraSPARC IIIi-based multiprocessor systems
• Generate system reset
• Binary compatibility with Solaris and I/O Drivers
UltraSPARC IIIi 4-way SMP

All JBus signals routed through repeater other than arbitration requests
Arbitration requests point to point (duplicate outputs) and not routed through repeater

64/32 bit, 66/33 MHz PCI buses (four)
JBus Features

- 16 byte split transaction shared address/data bus
  - Operating speeds up to 200 MHz
  - Peak bandwidth of 3.2 GB/s
- On-chip MOESI protocol with decoupled cache snooping
- Distributed round-robin arbitration favoring last port driver
- Low pin count (179 DTL signals)
- Support for out-of-order data return to source
- Simple point-to-point snoop result propagation
- Separate flow control (encoded) for address and data
- Parity protection for data and control
- Globally synchronous clocking
JIO Interface/Data Flow View

**PCI:**
- 64/32-bit@ 66/33 MHz
- 3.3 V (5 V tolerant)
- Support for 8 external masters

**JBus:**
- 16 byte data @ 120-200 MHz
- 1.5 V DTL (Dynamic Termination Logic)

**UPA64S:**
- 64-bit @ 120-200 MHz
- 3.3 V
- Support for 4 external masters

**JTAG**: 3.3 V

**MISC**: 3.3 V

**Encoded Interrupts**: 3.3 V

**Bypass**
# Clock Domain Details

<table>
<thead>
<tr>
<th>System Interfaces</th>
<th>Clock Domains</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>JBus</strong>: 1.5 V DTL</td>
<td>JBus PLL with PECL differential JBus system clocks as reference</td>
</tr>
<tr>
<td>16 byte bit shared address/data</td>
<td>100 – 200 MHz lock /operation range</td>
</tr>
<tr>
<td>120 – 200 MHz clock 179 signal pins</td>
<td></td>
</tr>
<tr>
<td><strong>Primary PCI</strong>: 3.3 v (5 v tolerant) LVTTL</td>
<td>Primary PCI PLL with single ended full range swing PCI reference clock signal</td>
</tr>
<tr>
<td>64/32 bit shared address/data</td>
<td>25 – 66 MHz lock range</td>
</tr>
<tr>
<td>25 – 66 MHz clock 103 signal pins</td>
<td>100 – 133 MHz range of operation</td>
</tr>
<tr>
<td><strong>Secondary PCI/UPA 64S Graphics</strong>:</td>
<td>Graphics PLL which can be selectively configured as:</td>
</tr>
<tr>
<td>3.3 v LVTTL</td>
<td>PCI : Single ended full range swing PCI reference clock signal</td>
</tr>
<tr>
<td>113 signal pins multiplexed</td>
<td>25 – 66 MHz lock range</td>
</tr>
<tr>
<td>PCI : 25 – 66 MHz clock</td>
<td>100 – 133 MHz range of operation</td>
</tr>
<tr>
<td>UPA : 120 – 200 MHz clock</td>
<td>UPA : PECL differential UPA system clock as reference</td>
</tr>
<tr>
<td></td>
<td>100 – 200 MHz lock /operation range</td>
</tr>
</tbody>
</table>
JBus Unit

- Provides JIO's interface to JBus
- Operational frequency of up to 200 MHz
- Responds to CPU snoops in 3 JBus cycles for all cases other than invalidates
- Maintains a copy of I/O cache tags
- Peer-peer arbitration ONLY at JBus level
- Supports up to 4 outstanding reads per cache
I/O Cache Unit

- Serves as prefetch buffer fully coherent with main memory
- Fully set associative cache memory of 8 lines of 64 bytes
- Maximum operational frequency of 133 Mhz
- Uses Read-Modify-Write /Write-back write policy for < 64 byte writes
- Bypasses cache to memory for 64 byte (cache line) writes
- FIFO-like counter-based replacement policy
- CSR-enabled prefetch of 1,2,3 cache lines for PCI commands
- CSR-enabled prefetch stride of 1 - 127 cache lines within 8K page
- Prefetch both on a hit or miss
JBus – I/O Cache Coherency

Snoop and read data return logic

Sync

j_tag_up_arb

Fill req

Snp req

Snp gnt

fill_gnt

wr_en

Mux

syn_jbus_tag_updt_dn

offset, state(snp)

address, offset, state(fill)

JBus side tag (T1)

“tag_updt_info” fifo (5 x 45)

Empty

Rd en

Cache control logic

Cache side tag (T2)

JBUS DOMAIN (200 MHz)

CACHE DOMAIN (133 MHz)

jbus_tag_updt_dn

Emptyjbus_tag_updt_dn
PCI Unit

- Provides JIO's interface to industry-standard PCI bus (2.2 spec)
- Internally Breaks up DMA transactions at 64 byte (cache line) boundaries
- Two-level low and high priority round-robin PCI bus arbitration scheme
- CSR - enabled prefetch of 1 cache lines for PCI commands
  - Two-cache line deep data buffer enhances DMA read performance
UPA Interface Unit

- Provides JIO's interface to Sun UPA64 system bus
- Enhanced Sun 2.0 Unified Port Architecture
- Master interface only
- Operational speed of 100 to 200 Mhz (UPA64S clock domain)
- Maximum of 16 total outstanding transactions
  - Up to 4 reads and 12 writes
  - Up to 16 writes (no reads)
**JIO Performance**

- 2 GB/s system I/O bandwidth (with 2 JIO chips)
- Uninterrupted reads and writes from PCI cards (64-bit/66 MHz!)
- Peak PCI performance for short bursts (32 or 64 bytes)
- UltraSPARC IIIi can saturate PCI and UPA with PIO stores (4, 8, 16, 64 bytes)
- Hardware table walk for IOMMU miss

### PCI DMA, 64-bit @ 66 MHz, 1 master

<table>
<thead>
<tr>
<th>Burst Size (bytes)</th>
<th>DMA write (MB/s)</th>
<th>DMA read (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>301</td>
<td>162</td>
</tr>
<tr>
<td>64</td>
<td>384</td>
<td>248</td>
</tr>
<tr>
<td>128</td>
<td>444</td>
<td>281</td>
</tr>
<tr>
<td>1024</td>
<td>515</td>
<td>465</td>
</tr>
<tr>
<td>8192</td>
<td>515</td>
<td>465</td>
</tr>
</tbody>
</table>

### PCI Memory PIO, 64-bit @ 66 MHz

<table>
<thead>
<tr>
<th>Burst Size (bytes)</th>
<th>PIO write (MB/s)</th>
<th>PIO read (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>88</td>
<td>62</td>
</tr>
<tr>
<td>8</td>
<td>106</td>
<td>106</td>
</tr>
<tr>
<td>16</td>
<td>211</td>
<td>211</td>
</tr>
<tr>
<td>64</td>
<td>384</td>
<td>384</td>
</tr>
</tbody>
</table>

### UPA Store Throughput, JBus @ 200 MHz

<table>
<thead>
<tr>
<th>Burst Size (bytes)</th>
<th>UPA Bus Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>200 MHz (MB/s)</td>
</tr>
<tr>
<td>8</td>
<td>1.55</td>
</tr>
<tr>
<td>16</td>
<td>1.50</td>
</tr>
<tr>
<td>64</td>
<td>1.32</td>
</tr>
</tbody>
</table>
JIO Implementation

- ASIC Gate Count : 922 K
- Memory Storage : RA - 55 K, Flops – 29 K
- Die Size : 9.5 mm. sq.
- Signal Pins : 433
- Package : 728 pin FCPBGA
- Max. Power Consumption : 10 Watts
- Technology : 0.25 Micron CMOS
Q & A