The BCM2132 GSM/GPRS Handset Baseband ASIC with Integrated EDGE and Media Functions

Nelson Sollenberger  
Li Fung Chang  
Paul Lu
BCM2132 Capabilities

- Four-slot EDGE/GPRS airlink for high-speed data communications at over 200 kbps
- Low-overhead incremental redundancy architecture
- VGA and 1.3 megapixel digital camera interface
- 18-bit color LCD display interface
BCM2132 Integration

- ARM9 microprocessor with 8k/8k caches & 16k/16k tcm’s
- Teaklite DSP
- NOR/NAND/SRAM/SDRAM support
- Hardware Acceleration for equalization, channel coding & ciphering
- Mixed signal for audio and modem interfaces
- GSM FR/EFR/HR/AMR + echo canceling & noise suppression
- Dedicated VGA or 1.3 Mpix camera interface
- Graphics Engine & color LCD support
- DMA controller
- MMC, USB, and stereo DAC interfaces
BCM2132: Outline

- EDGE overview
- EDGE implementation
- Incremental Redundancy functions
- Media functions
EDGE Best-Effort Data Airlink

- Evolution of GPRS airlink for high-speed data applications
- Adaptive modulation/coding
- Incremental redundancy
- Up to 3x the bitrate of GPRS for best effort data
- 8-PSK/GMSK at 271 kbps in 200 KHz RF channels
- Supports 9 modes at 8.8 to 59.2 kbps per time slot
- Supports peak rates over 200 kbps with 4 time-slots
## EDGE Airl ink
### Multi-mode Air Interface

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Modulation</th>
<th>Maximum rate [kb/s]</th>
<th>Code Rate</th>
<th>Blocks per 20 ms</th>
<th>Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCS-9</td>
<td>8PSK</td>
<td>59.2</td>
<td>1.0</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>MCS-8</td>
<td></td>
<td>54.4</td>
<td>0.92</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>MCS-7</td>
<td></td>
<td>44.8</td>
<td>0.76</td>
<td>2</td>
<td>B</td>
</tr>
<tr>
<td>MCS-6</td>
<td></td>
<td>29.6 / 27.2</td>
<td>0.49</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>MCS-5</td>
<td></td>
<td>22.4</td>
<td>0.37</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>MCS-4</td>
<td>GMSK</td>
<td>17.6</td>
<td>1.0</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>MCS-3</td>
<td></td>
<td>14.8 / 13.6</td>
<td>0.80</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>MCS-2</td>
<td></td>
<td>11.2</td>
<td>0.66</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>MCS-1</td>
<td></td>
<td>8.8</td>
<td>0.53</td>
<td>1</td>
<td>C</td>
</tr>
</tbody>
</table>
EDGE Traffic Channel Performance

![Graph showing BLER vs SIR for different Modulation schemes: GMSK, 8PSK, TU3 no FH.](image)
EDGE Traffic Channel 1 RX-slot Throughput

Throughput, kbps vs. SIR (dB) for different modulation and coding schemes (MCS).

- MCS-1 (R=1/2)
- MCS-2 (R=2/3)
- MCS-3 (R=6/7)
- MCS-4 (R=1)
- MCS-5 (R=3/8)
- MCS-6 (R=1/2)
- MCS-7 (R=3/4)
- MCS-9 (R=1)
Example: Coding and Puncturing for MCS-3

Rate 1/3 convolutional coding

3 bits

36 bits

316 bits

USF  RLC/MAC  Hdr.  HCS  FBI  E  Data = 37 octets = 296 bits  BCS  TB

948 bits

12 bits

108 bits

Rate 1/3 convolutional coding

puncturing

puncturing

SB = 12

12 bits

68 bits

372 bits

372 bits

372 bits

12 bits

68 bits

372 bits

372 bits

372 bits

P1

P2

P3

464 bits
Incremental Redundancy (IR)

- Send redundancy *only if* necessary
- Generalized Type-II ARQ
- Example

<table>
<thead>
<tr>
<th>Attempt</th>
<th>Data</th>
<th>Parity</th>
<th>Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st attempt</td>
<td></td>
<td></td>
<td>Rate 1</td>
</tr>
<tr>
<td>2nd attempt</td>
<td></td>
<td></td>
<td>Rate 1/2</td>
</tr>
<tr>
<td>3rd attempt</td>
<td></td>
<td></td>
<td>Rate 1/3</td>
</tr>
</tbody>
</table>

Transmitter | Receiver
EDGE Processing

• **ARM9 at 78/104 MHz supports:**
  – Protocol stack
  – L1 – physical layer control
  – Incremental redundancy control

• **Teaklite at 78 MHz supports:**
  – Equalizer preprocessing and control
  – RX data formatting
  – TX formatting and hardware control
  – Power control
  – Gain, frequency and time tracking
  – Measurements of desired and neighbor signals
EDGE Accelerators

- **Message Processor for channel coding on ARM9**
  - Supports all EDGE modes
  - Supports 4 slot RX operation

- **MAP Equalizer for 8PSK & MLSE for GMSK on DSP**
  - Provides robust performance for all EDGE/GSM modes
  - 3 stage for 8PSK: Feed Forward, Viterbi, & DFE

- **GMSK/8PSK modulator**
  - 4.3 MHz sampling minimizes analog requirements
  - GMSK & 8PSK are software selectable
Processor Performance

- About 10 MIP’s per RX time-slot required on DSP
  - Equalization performed in dedicated accelerator

- About 2 MHz per RX time-slot required on ARM9 for the IR functions
  - Channel decoding performed in dedicated accelerator

- Equalizer and Channel coding accelerators are pipelined with DSP and ARM9 processing for multi-slot reception

- About 10 MHz per RX time-slot on ARM9 for protocol stack and L1
BCM2132 IR Module Arch

- Place IR & channel coding on ARM9 + message processor channel coding accelerator
  - Order of 1 Mbit of IR memory is placed as a dedicated part of ARM’s external SRAM

- Minimize/avoid IR messaging between layers

- Tightly coupled IR control processing with block combining, header & data decoding & IR memory management under L1:
  - Optimize real-time performance
  - Shield RLC from IR hardware/memory detail
L1 Function

• Perform IR
  – IR control, IR memory management, header interpretation for combining
  – Deinterleave, Depuncture, combine, decode performed in hardware

• Maintain needed ARQ states for IR
  – IR module will track receiving state number and received block bit map
  – No extra messages are needed since RLC will automatically be synchronized by receiving correctly decoded data blocks

• Any correctly decoded headers as well as data blocks are passed to RLC/MAC
Incremental Redundancy Architecture

- ARM9
- RLC
- MAC
- L1
- Teaklite DSP
- PHY
- IR Control Software
- IR Memory
- Channel Coding Accelerator
BCM2132 Camera System

BCM2132

SRAM
FLASH

SF
FM

AHB

LCDC

18-bit Color LCD

DMA

VGA or MPIX CAMERA

CAM

ARM926EJ

I
D

AP
B

Copyright 2003 Broadcom Corporation. All Rights Reserved.
Camera Interface

- VGA or 1.3 Mpix support
- Internal line buffering
- YUV to RGB conversion
- Dithering
- Zooming & block selection
- DMA interface
LCD Interface

- Internal buffering for high performance & lower ARM9 overhead
- Up to 18-bit color
- Color expansion with programmable palette function
- Color dithering
- DMA interface, including link list support for very low overhead viewfinder mode & image capture
Conclusion

• BCM2132 is first baseband ASIC with 4-slot EDGE capability and supports over 200 kbps RX

• Integrated Mpix camera & color LCD modules and ARM9 computing support single chip multimedia GPRS/EDGE handset solutions

• Hardware acceleration for complex 8-PSK equalization and channel decoding supports very low MIPs in the DSP and saves power

• Incremental Redundancy architecture reduces inter-module signaling, reduces overhead, & supports simple use of external SRAM for the large required buffers