Broadcom WLAN Chipset for 802.11a/b/g

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Broadcom Corporation, CA, USA
Outline

• **Transceiver Architecture**
  – Baseband IC (BCM4306)
  – .11g RFIC (BCM2050)
  – .11a RFIC (BCM2060)

• **System Measurement Results**

• **Conclusion**
Single-band MiniPCI Card

BCM2050

BCM4306
Outline

• Transceiver Architecture
  – Baseband IC (BCM4306/9)
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DSSS/CCK PHY

- Microcoded preamble processor computes equalizer coefficients on each received frame.
  - > 170 MMACs/sec.
- 11 Mbps r.m.s. delay spread tolerance > 200 nsec.
BCM4306/9 AFE Diagram

DSSS/CCK BB
  | re-samp
  | re-samp
  | re-samp
  | MUX
  | BUF
  | 2x 8b ADC
  | 8b DAC
  | 8b DAC
  | RSSI ADC
  | PLL
  | BCM2050

OFDM BB
  | MUX
  | MUX
  | BUF
  | 2x 8b ADC
  | 8b DAC
  | 8b DAC
  | RSSI ADC
  | BCM2060

DEMUX

MUX

ADMUX

2x 8b ADC

8b DAC

8b DAC

6

DACs

switch
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BCM2050 Block Diagram
802.11b/g Transmitter Architecture

- Direct-conversion: Low-power, highly integrated
802.11b/g Receiver Architecture

- **Low-IF**: Power-hungry IF filters
- **Super-heterodyne**: Off-chip IF filters
- **Direct-conversion** is the best
**Receiver Front-End**

- Common-source LNA
- Gilbert-type I/Q mixers
- Active RC filters
- $S_{11}<-16$ dB, IIP3=-8 dBm

![Diagram of Receiver Front-End](image)

Normalized in-band gain, dB

5 dB/div (narrow mode)
Programmable RX Filter

Date: 9.MAY.2002 04:12:01
• 5\textsuperscript{th} order Chebychev LPF with programmable bandwidth has sharp cut-off to attenuate interference

• Two independent offset cancellation loops for LPF and PGA
Built-in Radio Calibration

- Built-in calibration ensures repeatability and consistency
  - Controls the effects of process variation to achieve the highest yield on a bulk CMOS process
  - Minimizes the effects of temperature variations during operation
- Calibrates all major blocks of the radio to within 2% of target
  - Filter phase and gain characteristics
  - Gain blocks and matching between major components
  - Center Frequency
  - Does not affect the normal operation and occurs in the normal Tx to Rx switching time – within 10 μsec.
Clock Generator Architecture

- Resolves PA pulling
- Spurs attenuated by on-chip LC filters
BCM2050 Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>4 dB typ.</td>
</tr>
<tr>
<td>Receiver IIP3 (max. gain)</td>
<td>-16 dBm typ.</td>
</tr>
<tr>
<td>Receiver IIP3 (min. gain)</td>
<td>4 dBm typ.</td>
</tr>
<tr>
<td>Transmitter output power</td>
<td>5 dBm typ.</td>
</tr>
<tr>
<td>Transmitter OIP3</td>
<td>18 dBm</td>
</tr>
<tr>
<td>Transmitter output power range</td>
<td>5 dBm to -15 dBm typ.</td>
</tr>
<tr>
<td>Transmitter EVM</td>
<td>-27 dB min. at 54 Mbps</td>
</tr>
<tr>
<td>Receive-mode current consumption</td>
<td>110 mA typ. (1.8 V)</td>
</tr>
<tr>
<td>Transmit-mode current consumption</td>
<td>80 mA typ. (1.8 V)</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>
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802.11a Radio Architecture

• Goal: Lowest Cost, Highest Performance, Lowest Power Consumption Radio
  – Direct Conversion Receiver and Transmitter Architecture
  – CMOS Implementation
  – Integrated PA
  – Take Advantage of Auto-Calibration Schemes
Implementation Challenges

• Direct Conversion:
  – DC offsets
  – Flicker noise on receive path
  – Rx path and/or Tx path oscillations
  – Quadrature accuracy
  – LO pulling
  – LO feedthrough

• Integrated PA
  – High linearity requirements for PA

• Auto-Calibration
  – Automatic Carrier Frequency Control (AFC) Loop
BCM2060 Simplified Radio Architecture

Balun → Balun
Balun → Balun

Optional BPF

SW

LO Generation

PLL

XO

AFC

TX Baseband

RX Baseband

JTAG

4 wires JTAG

Crystal Clock out

AFC_I in

AFC_Q in

TX_I in

TX_Q in

RX_I out

RX_Q out

RSSI’s out

Sensors out

RC & R calibration
Receiver Description

- Full integration
- On-Chip LNA input matching
- High-gain, low-noise, high-linearity, gain controllable LNA/mixer
- 3 stages of high-pass VGA’s
- A$5^{th}$-order Chebychev LPF
- Dual RSSI’s
- System NF of 4dB and max gain of 93dB is achieved
Transmitter Description

- Full integration
- 3rd-order Butterworth LPF’s
- Baseband and RF VGA’s
- High-linearity, high-power integrated class AB power amplifier
- On-chip power amplifier output matching
- $TX_{P_{-1dB}}$ of 19dBm and $P_{sat}$ of 23dBm are achieved
PLL Description

- Full Integration
- Integer-N PLL with programmable loop bandwidth
- "Fractional-VCO† with $f_{vco} = \frac{2}{3} f_{rf}$
  - Reduces pulling from high-power on-chip PA
  - Reduces transmitter LO feed-through
  - Reduces receiver DC offsets due to self-mixing
- Automatic frequency control integrated into PLL
- PLL achieves PN of $<-100\text{dBc/Hz} @ 30\text{KHz}$ offset with $f_{rf} = 5.24 \text{ GHz}$

†H. Darabi, et. al., ISSCC 2001
Chip Level Auto-Calibration

- VCO tuning
- AFC
- AFC self-calibration
- R-Calibration on bandgap blocks
- RC time constant calibration
- Integrated power detector
- Integrated temperature sensor
- Transmit LO feedthrough cancellation
Rx System NF and Sensitivity

**Graph 1:**
- **BB Frequency [MHz]:** 0.1, 1, 10
- **NF [dB]:** 2, 4, 6, 8, 10
- **Gain [dB]:** 0.1, 1, 10

**Graph 2:**
- **Data Rate [Mbps]:** 0, 20, 40, 60
- **Rx Sensitivity [dBm]:** -100, -95, -90, -85, -80, -75, -70, -65, -60
- **Measurement:** 11.7dB (σ = 0.3dB)
- **Spec:** 8.9dB (σ = 0.4dB)
Measured Transmit Output Power

- Saturated power limited
- EVM limited
- Spectral mask limited
Measured TX Power Spectrum

12.8dBm, 54Mbps, QAM64 (EVM Limited)

18.7dBm, 36Mbps, QAM16 (Spectral Mask Limited)
## Summary of Transceiver Performance

<table>
<thead>
<tr>
<th></th>
<th>Measured (this paper)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Band</strong></td>
<td>5.15 – 5.35 GHz</td>
<td>GHz</td>
</tr>
<tr>
<td><strong>RX NF</strong></td>
<td>4</td>
<td>dB</td>
</tr>
<tr>
<td><strong>RX Sensitivity (6Mbps)</strong></td>
<td>-93.7 ± 0.9 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX Sensitivity (54Mbps)</strong></td>
<td>-73.9 ± 1.2 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX IIP3</strong></td>
<td>-4.8 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX IIP2</strong></td>
<td>&gt; 30 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>RX Gain Range</strong></td>
<td>15 to 93 dB</td>
<td>dB</td>
</tr>
<tr>
<td><strong>TX Power Range</strong></td>
<td>-30 to +18.7 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>TX Psat</strong></td>
<td>+23 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>TX P-1dB</strong></td>
<td>+19 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td><strong>Vdd</strong></td>
<td>1.8 V</td>
<td>V</td>
</tr>
<tr>
<td><strong>Vdd_PA</strong></td>
<td>3.3 V</td>
<td>V</td>
</tr>
<tr>
<td><strong>Phase Noise @ 30KHz</strong></td>
<td>-100 dBc/Hz</td>
<td>dBC/Hz</td>
</tr>
<tr>
<td><strong>RX Power Consumption</strong></td>
<td>150 mW</td>
<td>mW</td>
</tr>
<tr>
<td><strong>TX Power Consumption</strong></td>
<td>380 (15dBm OFDM output) mW</td>
<td></td>
</tr>
<tr>
<td><strong>ESD</strong></td>
<td>&gt; ±2.5 on all pins</td>
<td>KV</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>0.18um 1P5M CMOS</td>
<td></td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>11.7 (including padring) mm²</td>
<td></td>
</tr>
</tbody>
</table>
Die Microphotograph of BCM2060
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Flat-Channel Sensitivity Test Diagram

REFERENCE (Transmitter) → RF mux ↓ Power Meter → DUT (Receiver)

Dir. Coupler ↔ Prog. Atten. ↔ Dir. Coupler
802.11g System Sensitivity Test Result

1 Mbps sensitivity
-97 dBm

54 Mbps sensitivity
<-70 dBm

Results include all PCB and connector losses.
Measured BCM2060 Phase Noise

Residual PM = 0.0075 rad = 0.43 deg

From 1 kHz
To 305.8116 kHz

Target Specifications
Measured 802.11a TX Constellation Diagram

EVM = -33dB
Po = +6dBm
64-QAM
54 Mbps
Measured 802.11a TX EVM Histogram

EVM = -33dB
Po = +6dBm
64-QAM
54 Mbps
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Conclusions

• Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11g Transceiver Reported to Date
  – 4 dB Rx chain noise figure
  – Excellent performance in the presence of real-world impairments
  – Fully integrated, direct conversion
  – Various integrated self contained or system level calibration capabilities for high yield and tight tolerances
  – 790 mW transmit or receive (1.8 V), RF and baseband/MAC
  – 10 mW sleep mode, RF and baseband/MAC
  – 802.11g receiver sensitivity with all board losses
    • -70 dBm 54 Mbps
    • -97 dBm 1 Mbps
Conclusions

• Highest Performance, Highest Integration, Smallest Size, Lowest Power Consumption IEEE 802.11a Transceiver Reported to Date
  
  – 4 dB Rx chain noise figure
  
  – 23 dBm Tx $P_{\text{sat}}$ with integrated PA
  
  – Excellent performance in the presence of real-world impairments
  
  – Fully integrated, direct conversion
  
  – Integrated or system level calibration capabilities for high yield and consistent performance
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