A UMTS Baseband Receiver Chip for Infrastructure Applications

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Outline

- UMTS/CDMA Cellular System Overview
- CDMA Base Station Receiver Functions
- System Partitioning
- The TCI110 Receive Chip-rate Application Specific Signal Processor (ASSP)
  - Correlator architecture
  - Front-end buffer
  - Finger de-spreader
  - Path searcher
  - Preamble detector
  - Host Interface
- Summary
Cellular System

Base Station (Node B)

Uplink (reverse link)

Downlink (fwd link)

User Equipment (UE)
UMTS FDD 3G Standard

- Frequency Division Duplex
- Wideband CDMA
- Variable data rates and associated services
  - 2 MBPS peak rate
- Network backward compatible to GSM
3G Base Station: Key Care-abouts

Cost per channel

Flexibility

- Variable data rate and traffic
  - Mix of rates from 12.2Kbps (voice) up to 2Mbps (data)
- Flexible cell sizes
  - Macro/Micro/Pico/In-door
- Support of disparate environments
  - Vehicular, pedestrian, stationary
- Flexible resource allocation
  - Seamless processing/memory trade-off between various traffic scenarios
- Flexible implementation of base-band algorithms
  - Allow for field upgrades/enhancements
UMTS/W-CDMA Deployment Projections

Region

- **Japan**: Prototype 2001, Commercial 2003

Time

- 2001
- 2002
- 2003
- 2004
- 2005
Spread Spectrum

Pseudo-Noise (PN) Sequence

User Data “001...”

\[ X \]

\( N \) “chips”

“0” \quad “0” \quad “1”

Bandwidth \( w \)

Bandwidth \( Nw \)
CDMA

: PN sequences for different users are orthogonal

\[ \sum_{k} P_{N_i}(k) P_{N_j}(k) \approx 0 \]

: “De-spread” with local PN sequence
Base Station Receiver Functions

RF Front End Analog Baseband

Despreaders
RAKE fingers

Preamble Search

Multi-Path Search

Parameter Estimation and Control
- Channel estimation
- AFC, AGC, Time Tracking
- Measurements
- Finger allocation
- TFCI decoding
- RACH post-processing

Multipath Combining

Symbol Rate Processing
- Channel decoding
- Rate matching
- CRC
- De-interleaving
- Channel de-mux

Radio Resource Management

Network Interface

Network Backplane

Digital Baseband

Real World Signal Processing™

Texas Instruments
Chip-Rate Processing Front-End

De-spreader functions

- Implements Rake “fingers”
- Inner product function:

\[
y(k) = \sum_{n=0}^{SF-1} x(k.SF + n) * pn(k.SF + n)
\]

Search functions

- Path search and Preamble search
- Search for pilot signal within a time window of uncertainty
- Matched filter function:

\[
y(k) = \sum_{n=0}^{M-1} x(k-n) * pn(n)
\]

Very high computation rates involved

- > 150 Billion Complex “Multiply Accumulates” per second
- Relatively low processing rate downstream of the correlator
System Partition

TCI110

Receive Chip-Rate ASSP

DSP

TCI100

Chip-Rate Assist DSP

DSP

TCI100

Symbol-Rate DSP

DIGITAL BASEBAND

DESPREADERS
RAKE fingers

PREAMBLE SEARCH

MULTI-PATH SEARCH

RADIO RESOURCE MANAGEMENT

MULTIPATH COMBINING

PARAMETER ESTIMATION AND CONTROL

- Channel estimation
- AFC, AGC, Time Tracking
- Measurements
- Finger allocation
- TFCI decoding
- RACH post-processing

SYMBOL RATE PROCESSING

- Channel decoding
- Rate matching
- CRC
- De-interleaving
- Channel de-mux

NETWORK INTERFACE

REAL WORLD SIGNAL PROCESSING™

TEXAS INSTRUMENTS
TCI110 Architecture

TCI110

FE

Front-End Interface

Power Estimator

ARMP

Preamble Detector

Path Monitor

ARMF

Finger Despreaster

Synchro module

Host Interrupt Interface

Host Transfer Interface

TCI100

R E A L  W O R L D  S I G N A L  P R O C E S S I N G ™
Correlator Architecture

Four task-based accelerators

- Finger de-spreader, Path monitor, Preamble detector, and Power estimator
- Tasks set-up through software running on a programmable DSP
- Results transferred to DSP periodically via DMA

Each accelerator employs a vector-correlator architecture

- Datapath and control customized for specific functions (FD, PM, PD, PE)
- Control includes two ARM micro-controllers
- All tasks mapped to a accelerator run on the same data path in a time-multiplexed manner
Correlator Architecture

Front End Interface

Input buffer: 8x Oversampling N antennas

PN Code Gen

Adder Trees

Coh. ACC

Non-coh. ACC

Scratch Mem.

Scratch Mem.

Output Memory

From the Analog Front End

Control Memory

ARM Microcontroller

Task Buffer

TCI API

DSP Control S/W
Front-End Interface

Function

- **Distribute**
  - Up to 24 sample streams (including 2 delay streams to FD)

- **Interpolate for FD**
  - From 8x, or 4x, or 2x samples/chip to 8x samples/chip

- **Decimate for other modules**
  - From 8x, 4x, 3x samples/chip to 2x for PD and PM and 1x for PE

Typical configurations:

<table>
<thead>
<tr>
<th>Bus Mode</th>
<th>Oversampling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td>16 bits</td>
<td>12</td>
</tr>
<tr>
<td>32 bits</td>
<td>24</td>
</tr>
<tr>
<td>48 bits</td>
<td>24</td>
</tr>
</tbody>
</table>
Finger De-Spreader

Performs de-spreading of received multi-path components in a CDMA RAKE receiver
- Data/Control channel despreading
- Includes Early/On-time/Late-time de-spreading with energy accumulation for time tracking
- Flexible allocation of a pool of correlation resources

Usage scenarios:

<table>
<thead>
<tr>
<th>Finger Despreader</th>
</tr>
</thead>
<tbody>
<tr>
<td>SF</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>256</td>
</tr>
<tr>
<td>128</td>
</tr>
<tr>
<td>64</td>
</tr>
<tr>
<td>32</td>
</tr>
<tr>
<td>16</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>4</td>
</tr>
</tbody>
</table>
Finger De-Spreader Usage Examples

- 2048 chip-rate de-spreaders running in parallel
- May be flexibly configured in a number of ways
  - 64 UE at 12.2Kbps, 8 Fingers/UE
    - DPDCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking
  OR
  - 128 UE at 12.2Kbps, 4 Fingers/UE
    - DPDCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking
  OR
  - 51 HSDPA UE, 8 Fingers/UE
    - ADPCH de-spreading
    - HS-DPCCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking
  OR
- Combinations of the above within the 2048 de-spreader limit
Path Monitor Performance

Performs multi-path search for all received users

- Flexible time-multiplexing of resources among users
- Includes flexible coherent and non-coherent (energy) accumulation

Typical usage:

- 64 Users, Search over 2 antennae in parallel
- 128 chip window (at ½ chip resolution), 1/8th activity factor

Other usage scenarios:

<table>
<thead>
<tr>
<th>Total UEs</th>
<th>UEs</th>
<th>Activity</th>
<th>Search Window</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Chips</td>
</tr>
<tr>
<td>44</td>
<td>8</td>
<td>1/2</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>1/1</td>
<td>128</td>
</tr>
<tr>
<td>24</td>
<td>16</td>
<td>1/2</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>1/1</td>
<td>128</td>
</tr>
<tr>
<td>12</td>
<td>8</td>
<td>1/1</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>1/1</td>
<td>256</td>
</tr>
</tbody>
</table>
Preamble Detector Performance

Implements a sliding window correlator for detection of Random Access Channel Preamble

- Flexible coherent and non-coherent accumulation intervals
- Parallel search over all 16 RACH signatures

Typical usage

- Correlate over complete preamble (4096 chips)
- 512 chip window, \( \frac{1}{2} \) chip resolution (20Km cell radius)
- Search over 2 antennae in parallel

Other usage scenarios:

<table>
<thead>
<tr>
<th>Scr. Codes</th>
<th>Signatures</th>
<th>Activity</th>
<th>Search Window</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Chips</td>
</tr>
<tr>
<td>2</td>
<td>16</td>
<td>1/2</td>
<td>1024</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>1/1</td>
<td>512</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>1/2</td>
<td>256</td>
</tr>
</tbody>
</table>
Host Interface

TCI110

Configuration/Status
Registers & Tables

Output buffers
(Symbols, EOL, Search data)

TCI100

CPU

EMIF A

L2

EDMA Controller And PaRAM

Step 1:

Host Interface sets up EDMA channels in PaRAM

Step 2:

EDMA controller transfers data blocks to L2.
HI re-groups the data to have one transfer per user or groups of users
TCI110 Chip Metrics

- **Technology**: 0.13 μm CMOS, 7 Layer Metal, High speed copper process
- **Size**: ~ 75M Transistors, ~ 50% die area is SRAM, 35 x 35 388-pin BGA package
- **Clock**: ~ 125 MHz Datapath, ~ 250 MHz ARM
- **Power**: ~ 2W, 3.3 V I/Os, 1.2 V Internal
TCI110 Summary

- **Lowest cost per channel enabled via**
  - Time-multiplexed datapath architecture that allows memory sharing
  - Highly integrated SOC

- **Flexible / Programmable**
  - “Pool of Resources” concept for flexible resource allocation in a multi-channel context
  - Inherently flexible design enhanced with the programmability of embedded cores
  - Yet optimized for chip rate applications:
    - ~ 200 Billion chip operations per second
    - Parallel datapaths for finger de-spreading, path monitoring, preamble detection
    - Dedicated interface and distribution of antenna data
    - Highly optimized transfer of results data to C64x

- **Enhanced time-to-market**
  - Programmable approach allows bug fixing / feature enhancement in Software
Flexibility/Cost Combination of DSP + Custom ASIC

Channel Card Architecture Approach of Leading WI OEMs

- All DSP
- DSP + FPGA (Reconfigurable)
- TCI100 + Customizable ASSP
- All ASIC

New Single Platform Chipset is Customizable to Meet Each OEM’s Individual Needs
Customizable Chipset Maintains OEMs Ability to Differentiate

High-performance, programmable DSP

Flexible hardware configured via registers and commands under DSP software control