A Single Chip Shared Memory Switch with Twelve 10Gb Ethernet Ports

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Outline

• Background
• Overview and Features
• Switch Implementation
• Evaluation
• Summary
Background

- IP-based networks connect all the computing resources (All-IP).
- Ethernet protocol is commonly used for IP networks.
- 10Gb Ethernet is a promising solution for unified, fat pipe between servers and storage systems.

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Primary Target Applications

- Our primary target is infrastructure for computing platform, such as SAN, Clusters, Blade Servers.
- Those applications require short latency, low cost and high density.
  - Motivation to develop a dense 10Gb Ethernet switch.
- So, the design strategy is set as follows.
  - Focus on layer-2 switching.
  - High-throughput/low latency switch core.
  - SerDes integration for copper solution.

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MB87Q3050 Overview

- Twelve 10 Gb Ethernet ports.
- Integrated SerDes for XAUI.
  - 3.125Gbps x 4 lane/direction
- Layer-2 switching with 802.1Q VLAN.
- Output queue switching using shared memory.
- 240 Gbps shared memory bandwidth.
- Cut-through forwarding.
- Statistics counters for RMON.
Designing a Switch Core

- A protocol independent switch core was developed.
  - Credit based flow control.
  - Packet by packet operation, allowing variable length from 64B to 9KB.
    - This is not a fixed-length cell switch.
  - Four level priority queue, with simple distributed arbiters per output port.
  - Cut-through forwarding (fall-through latency of the core: 150ns)
  - Multicast support for “single copy, multiple read”.

![Switch Core & Shared Memory Diagram]
Input Buffering for Cut-Through

- The switch core is designed for cut-through forwarding of variable length frames.
  - The switch core has NO speed-up in terms of the bandwidth per port.
    - All the data path in the switch is running at 10Gbps data rate.
    - Popular implementation with crossbar switches may have increased B/W per port.
  - The switch core assumes NO fragmentation.
    - The entire packet should be transferred at 10Gbps rate.
  - These features are desired to handle variable length frames in Ethernet protocol, to minimize store&forward operation.
- Input buffering is simply for speed-matching between clock domains when cut-through mode is chosen.
On-chip Interconnect for Shared Memory

- An on-chip memory sub-system is designed for 12 10Gbps reads AND 12 10Gbps writes.
  - “Multi-port Stream Memory”
- Deep interleaved memory banks are connected via distributed, multi-stage interconnection network.
  - “No global arbitration” is a good policy for chip integration and timing closure.
- Switching is rescheduled at every packet boundary for access path arbitration.
- Arbitration delay exists between packets (as shown later).
Output Buffering for Short Latency

- Frames come out of the switch core without fragmentation, at 10Gbps rate.
- However, arbitration delay (caused by on-chip interconnect) exists between frames.
- The average value is 32 cycle (assuming random, full-loaded traffics).

- On the other hand, outgoing packets has 8 byte preamble and 12 byte IPG as defined in the Ethernet protocol.
  - 5 cycles between frames in the switch core.
- Thus, with a small amount of FIFO, it is possible to sustain wire-speed throughput.
  - We do not need a large FIFO. The size is much smaller than the maximum packet size.
  - It also helps to reduce the fall-through latency in a loaded condition.

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# Chip Implementation

## MB87Q3050
12-port, 10Gbps Ethernet Switch Chip

<table>
<thead>
<tr>
<th>Items</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>Fujitsu CS91: 0.11um CMOS ASIC</td>
</tr>
<tr>
<td>Logic</td>
<td>6.3M gates (total)</td>
</tr>
<tr>
<td>SRAM</td>
<td>897K Bytes (total)</td>
</tr>
<tr>
<td>Core Logic Frequency</td>
<td>312.5MHz</td>
</tr>
<tr>
<td>Package</td>
<td>FCBGA-728</td>
</tr>
<tr>
<td>Signals</td>
<td>336</td>
</tr>
<tr>
<td>High Speed IO</td>
<td>XAUI (3.125Gb/s x 4) X 12</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>15.3 W (typical), full-loaded</td>
</tr>
<tr>
<td>Die Size</td>
<td>16mm x 16mm</td>
</tr>
</tbody>
</table>

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Evaluation Board

- For functional validation
  - Hardware
  - Firmware
- Nine copper cable connectors.
  - Tested with copper cables up to 5m.
- Three optical Interfaces.
  - XENPAK modules.

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Performance: Zero-loss Throughput

- Zero-loss Throughput is measured using the *first-silicon*.
  - Optical links are used for 2-port paring configuration.
  - Optical links and Copper cables are used for full mesh configuration.
    - Slight packet loss is observed (to be fixed in future silicon).
Performance: Latency

- Fall-through latency at 100% throughput workload is measured with the first silicon.

<table>
<thead>
<tr>
<th>Packet size bytes</th>
<th>Cupper Cable</th>
<th>Optical Cable (w/ XENPAK modules)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>750</td>
<td>1160</td>
</tr>
<tr>
<td>128</td>
<td>670</td>
<td>1090</td>
</tr>
<tr>
<td>256</td>
<td>660</td>
<td>1190</td>
</tr>
<tr>
<td>512</td>
<td>630</td>
<td>1230</td>
</tr>
<tr>
<td>1024</td>
<td>670</td>
<td>1280</td>
</tr>
<tr>
<td>1280</td>
<td>640</td>
<td>1140</td>
</tr>
<tr>
<td>1518</td>
<td>630</td>
<td>1190</td>
</tr>
<tr>
<td>9216</td>
<td>660</td>
<td>1220</td>
</tr>
</tbody>
</table>
Application Prototype: 1Gb Switch Box

10G Switch Board
- Twelve 10G ports on switch backplane

1G Board
- 1G x 24 ports

10G Board
- 10G x 12 ports

Switch

6 boards: 1G or 10G board

Layer-2 switch for cluster systems by Fujitsu Laboratories Ltd. (Japan)

Flexible port configuration
Ex) 1G x 144 ports
10G x 12 ports

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Summary

• MB87Q3050 was designed for 10Gb Ethernet-based interconnection for servers and storage equipment.
  – Low cost, dense integration.
  – High-throughput, low latency.
• The switch achieves wire-speed operation at each port, by 240Gbps shared memory bandwidth.
• It also achieves 450ns latency with cut-through forwarding.

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THE POSSIBILITIES ARE INFINITE