The RM9150 and the Fast Device Bus High Speed Interconnect

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Agenda

- CPU-based SOC Design Challenges
- Fast Device Bus (FDB) Overview
- Generic Device Interface
- FDB Block Diagram
- Architectural Advantages
- Summary
Typical CPU-based SOC Building Blocks

- System bus architecture is becoming increasingly important
- CPU frequency increase must be matched by bus and memory speeds

SoC Design Issues

- Multiple clock domains needed
- Custom bus interface to each peripheral
- Little design re-use

Performance scalability issues
Typical Bandwidth of Various Blocks

<table>
<thead>
<tr>
<th>Block</th>
<th>Bus Width (GB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>0.25 GB/s</td>
</tr>
<tr>
<td>DDR Memory Controller</td>
<td>2.4 GB/s</td>
</tr>
<tr>
<td>Gigabit Ethernet MAC</td>
<td>0.25 GB/s</td>
</tr>
<tr>
<td>Gigabit Ethernet MAC</td>
<td>2.6 GB/s</td>
</tr>
<tr>
<td>Gigabit Ethernet MAC</td>
<td>2.5 GB/s</td>
</tr>
<tr>
<td>Gigabit Ethernet MAC</td>
<td>1.6 GB/s</td>
</tr>
</tbody>
</table>

Typical standard buses can't keep up with memory controller and other high-bandwidth peripherals.

Fast Device Bus / Generic Device Interface

- Common design interface for all peripherals
- GDI interface specification available to PMC customers
Fast Device Bus Features

- Central arbitration logic and physical address map
- Modular design, ports can be easily added and subtracted (2-12)

Fast Device Bus Features (cont.)

- 128-bits, multiplexed address and data
- Separate grant signal, addr./data grant per port
- 400 MHz – 500 MHz multiple master, shared on-chip bus
- 3-bit credit release bus, one per port connected from each port to the central arbiter
Central Arbiter Operation / Advantages

- Employs a two-stage arbiter
  - Request Bus Arbiter: Round robin priority
  - Second stage: Choose next owner of A/D bus based on request priority / target transaction resource availability
  - Both arbiters are pipelined, selecting a new owner every cycle

- The Central Arbiter is for efficient scheduling of main bus usage
  - Main bus is never granted unless the target can accept the transaction, therefore no “not acknowledges” and no “retries”

- The Central Arbiter guarantees fair access to high-contention targets

First Device Based on the FDB: RM9150

- Each port contains a fixed number of buffers to accept a fixed number of transactions
- Number of buffers optimized to meet each device’s specific performance requirements
- Built-in re- synchronization logic to support different frequency modes
- 128-bit GDI to FDB interface for DDR1/2 memory controller for optimum bandwidth

- FDB is implemented using a single core clock domain
FDB/GDI Methodology Greatly Reduces Verification Effort

- Only need to design new Intellectual Property (IP) blocks with GDI interface (or modify existing IP to support GDI)
- Once this IP with GDI interface has been verified, then this ensures that the IP block can communicate with the FDB and all devices connected through GDI to the FDB
- Without GDI / FDB, would need to design a custom interface to each IP block and verify that it can communicate with the system interconnect (for each peripheral device in the SOC)
- Solves an order \( n^2 \) verification problem by reducing it to an order \( n \) effort

RM9150 Feature Summary

- First PMC-Sierra SOC to implement the FDB/GDI
- E9000 processor (<500 MHz to 1GHz capability)
  - 64-bit, dual-issue, superscalar, 7-stage pipeline
  - 16KB L1 caches / 256KB L2 cache (parity, ECC)
- FDB Trace and Performance Monitor
- 8-bit 600 MHz DDR HyperTransport Bus v1.03
- Two 32-bit PCI buses, 66 MHz, v2.3
- 167MHz/ 200 MHz 64-bit DDRII SDRAM Controller
  - Up to 4GB of memory
- Two 10/100/1000 Ethernet MACs (802.3), TBI, GMII, MII
- 4-channel DMA controller
- Local Bus controller to external ROM, Flash, Compact Flash, PCMCIA, USB 2.0 devices
- Serial Communications Master Block
  - DUART, 2-wire interfaces, MDIO/MDC, 64 GPIO

896 BGA package
0.13um TSMC process
 PMC’s Solution: New Design Methodology
- Performance flexibility & quick-turn SOC designs

Fast Device Bus / Generic Device Interface Architectural Advantages

- GDI allows each peripheral to interface to FDB fully synchronously, semi-synchronously, or totally asynchronously, essentially eliminating global clocking issues
- Standard GDI interface allows development of re-usable IP blocks, ability to use different future bus interconnects
- GDI allows replacement of the interconnect behind it without re-designing the peripheral devices -> scalability
- Allows customers to integrate their IP or leverage PMC’s IP to quickly design complex SOC’s at various price/performance points
- Greatly reduces device verification effort (factor of n) for fast time-to-market
Summary

- Innovative Fast Device Bus / GDI bus architecture
  - Tuned for optimal performance (latency, bandwidth to critical peripherals)
  - High utilization due to efficient arbitration
  - Enables easy design re-use (common GDI interface)

- E9000 CPU and robust set of RM9150 peripherals address multiple market segments
  - Networking, Storage, Industrial Control, and High-end Printer and Consumer

- First instance of PMC’s platform-based high-performance, highly integrated SOCs using the FDB