SH-Mobile3: Application Processor for 3G Cellular Phones on a Low-Power SoC Design Platform

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Outline

- Background
- Chip overview
- Active power reduction
  - High MIPS/MHz CPU core
  - Java accelerator
- Standby power reduction
  - Low-power SoC design platform
  - Supply domains and two standby modes (Resume and ultra standby modes)
- Summary
Background

- **3G cellular phone**
  - High data throughput (144k – 2M bps)
  - Advanced applications (Java, videophone & 3D CG)
  - Long battery life (> 300 hours)

Advanced process technology

- Higher operating speed, large amount of integration and lower leakage power are conflicting requirements.

Chip overview

- 130-nm, Dual-Vth, Dual-tox CMOS (5Qu) technology
- Dedicated multiple computation engines:
  - SuperH CPU core (SH-X), inc. DSP & Java™ (BTU) engines
  - MPEG-4
  - 3D graphics
- 256-kB on-chip RAM (URAM)
- Low-power SoC design platform
  - μI/O (level shifter technology)
  - On-chip power switches (PSWs)
Active power reduction

To achieve sufficient performance with minimum operation frequency and power consumption,

- High MIPS/MHz CPU core
  - Optimized dual-issue 7-stage pipeline
- Dedicated multiple computation engines
  - Java accelerator
  - MPEG-4
  - 3D graphics
PipeLine structure

- Dual-issue 7-stage Pipeline
  - Higher MHz, but lower cycle performance
- Optimized pipeline using delayed execution enhances cycle performance.

Delayed execution starting points

<table>
<thead>
<tr>
<th>I1</th>
<th>I2</th>
<th>ID</th>
<th>E1</th>
<th>E2</th>
<th>E3</th>
<th>E4</th>
<th>E5</th>
<th>E6</th>
<th>E7</th>
</tr>
</thead>
</table>

Instruction Fetch
- Early Branch
- Decode
- Execution
- WB
- Address
- Data Load
- WB
- Tag
- -
- Data Store

CPU

Decode

Multiply

WB

ALU

WB

DSP

Delayed execution (DE)

- DE accelerates multiple-cycle and dependent Inst. flows.
- e.g. typical DSP instruction flow:
  - Load --- Arithmetic Executions --- Store

Conventional Architecture: 3-cycle Stalls

<table>
<thead>
<tr>
<th>Load:</th>
<th>E1</th>
<th>E2</th>
<th>E3</th>
<th>E4</th>
<th>E5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiply:</td>
<td></td>
<td>E1</td>
<td>E2</td>
<td>E3</td>
<td>E4</td>
</tr>
<tr>
<td>Store:</td>
<td>E1</td>
<td>E2</td>
<td>E3</td>
<td>E4</td>
<td>E5</td>
</tr>
</tbody>
</table>

Delayed Execution: No Pipeline Stall

<table>
<thead>
<tr>
<th>Load: MOVX.W @R4, X0</th>
<th>E1</th>
<th>E2</th>
<th>E3</th>
<th>E4</th>
<th>E5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiply: PMULS X0, A0</td>
<td>E1</td>
<td>E2</td>
<td>E3</td>
<td>E4</td>
<td>E5</td>
</tr>
<tr>
<td>Store: MOVX.W A0, @R5</td>
<td>E1</td>
<td>E2</td>
<td>E3</td>
<td>E4</td>
<td>E5</td>
</tr>
</tbody>
</table>
Performance evaluation

![Graph showing MIOPS/MHz performance evaluation]

Benchmark: Dhrystone 2.1

Operating power of processor core

![Graph showing operating power of processor core]

Benchmark: Dhrystone 2.1

V_DD = 1.2V

- 0.57 mW/MHz at 1.0V
- 0.40 mW/MHz at 1.8 MIPS/MHz

1.8 MIPS/MHz

0.40 mW/MHz

= 4500 MIPS/W
Java accelerator (BTU)

BTU block diagram
Parallel execution in BTU

- BTU shares control information and data with CPU. It enables parallel execution of data and control processing. (e.g. Java exception detection)

<table>
<thead>
<tr>
<th>Coprocessor type</th>
<th>Conv. accelerator</th>
<th>BTU</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>ALU</td>
<td>CPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cache</td>
<td>Cache</td>
<td>Cache</td>
</tr>
</tbody>
</table>

Data separated: Data shared: Control shared

Java power evaluation

- Performance: w/BTU 6.55 ECM/MHz (basic VM 0.64 ECM/MHz)
- Power consumption is reduced by 6%, and power/ECM is reduced by 90%.

![Power Consumption Chart]

Evaluation board 216 MHz, CLDC 1.0.4
Standby power reduction

To achieve lower standby power with minimum speed overhead,

- Low-Power SoC Design Platform
  - On-chip power switches (PSWs)
  - μI/O
  - Low leakage data-retention RAM technology
- Two Standby modes
  - Resume standby mode
  - Ultra standby mode

Low-power SoC design platform (PSWs)

- Thick-tox High-Vth NMOS transistors are used for on-chip power switches (PSWs).
- It minimizes various leakage currents such as subthreshold, gate tunneling, GIDL, and junction leakage.
Low-power SoC design platform (μI/O)

- μI/O has level-shift function and provides optimal supply & voltage domains for dedicated multiple computation engines.
- It also prevents invalid signal transmission and supports:
  - Internal vss1 and/or vss2 shutdown by on-chip power switches
  - External vdd1 and/or vdd2 shutdown by off-chip regulators

![Diagram of μI/O design platform]

Low-leakage data-retention memory

- Hierarchical on-chip power switches in SRAM provide subdivisional power-line control.
  - In active mode
    - Vssm, Vssa, Vssc = Vss
    - Vddw = Vdd (sel.) ~ 0.4 V down (unsel.)
    - Local Vss = Vss
  - In retention mode
    - Vssa, Vssc: Hi-Z
    - Vssm: ~ 0.4 V up
    - Vddw: ~ 0.4 V down
    - Local Vss = Vss
  - In shut-down mode
    - Local Vss: Hi-Z
Leakage current of the memory

![Graph showing leakage current comparison between conventional and proposed methods.](image)

- **Conventional**: Memory cell 920 µA, Word driver 700 µA, Amp -25%.
- **Proposed (in active)**: Memory cell 700 µA, Word driver 50 µA (95% reduction).
- **Proposed (in retention)**: Memory cell 50 µA (95% reduction).

256-kB, Room Temp. V_{DD} = 1.2 V

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Two low-power modes

- **Ultra standby**
  - Low leakage (~10 µA)

- **Resume standby**
  - Low leakage (~100 µA)
  - Quick recovery (<3 ms)

![Block diagrams showing Ultra and Resume standby modes.](image)
R-standby recovery operation

- Hardware operation
  - Power switch control
  - Clock generation (PLL, D.PLL lock)
  - Data backup using backup latch
    - BAR (Boot Address Register) holds restart address
    - Clock and interrupt setting needed just after wake-up

- Software operation
  - URAM: data backup mem.
  - Control registers
  - OS task table
  - etc.

Recovery time from R-standby

- Total recovery time from R-standby mode is only 1.6 ms or 2.8 ms (@Ext. clk=32 kHz).

- w/o D.PLL lock
- w/ D.PLL lock (Ext. CLK=32kHz)
Standby power consumption

Room Temp. \( V_{DD} = 1.2 \) V

Leakage current (\( \mu A \))

- Standby w/o power cutoff: 2.2 mA
- R-standby: 86 \( \mu A \)
- U-standby: 11 \( \mu A \)

-96% - 99%

Summary

- 130-nm 5-layer-Cu dual-Vth, dual-tox CMOS technology
- Dedicated multiple computation engines:
  - SuperH CPU core (SH-X) including DSP & Java\textsuperscript{TM} engines
  - MPEG-4
  - 3D graphics
- Power efficiency, SH-X: 4500 MIPS/W
  - Java: 6.55 ECM/MHz
- Low-power SoC design platform
  - On-chip power switches
  - \( \mu I/O \)
  - Low-leakage data-retention RAM
- Two standby modes (R-standby and U-standby)
  - Leakage current: 86 \( \mu A \) and 11 \( \mu A \)
  - Recovery time from R-standby: 1.6 ms or 2.8 ms (@Ext. clk=32 kHz)

RENESSAS

HITACHI

Inspire the Next