Digitally Assisted Analog Circuits

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Outline

• Motivation
  – Progress in digital circuits has outpaced performance growth in analog circuits by a large margin

• Digitally Assisted A/D Converters
  – Using digital computing capabilities as a new driver to improve A/D converter energy efficiency
  – Examples
    • Experimental proof-of-concept result
    • Next generation designs

• Conclusions
Modern Electronic Circuits

• Trend towards ubiquitous sensing, communication and computing
  – "Ambient Intelligence"

• Signal processing predominantly done in digital domain
  – Rapidly improving digital capabilities, fueled by "Moore's Law"

• Irreplaceable "bottleneck" - analog circuits
  – Analog-Digital Converters (ADCs)
  – Digital-Analog Converters (DACs)
  – Filters and amplifiers (Anti-aliasing, RF power amplification, …)

• Focus of this talk: ADCs
Issue 1: Throughput

* Performance measure: Bandwidth x Number of quantization levels
Issue 2: Power and Energy

• Example: Cell phone
  – Battery has roughly 3Wh of Energy
  – For a talk time of 12 hours, can draw no more than 250mW
  – Only a fraction of that power available for ADC

• In an increasing number of applications, key issue is how much performance you can squeeze into a fraction of 0.1…1Watt

• What is the trend in ADC versus digital power/energy consumption?
ADC Energy versus Digital Energy

- Interesting metric to look at
  - How many digital gates can you toggle for the energy needed in one A/D conversion?

- Example
  - Standard digital gates (NAND2) in 0.13mm CMOS consume about 6nW/Gate/MHz
    - Energy/Gate = 6fJ
  - State-of-the-art 10-bit ADC consumes 1mW/MSample/sec
    - Energy/Conversion = 1nJ
  - Energy equivalent number of gates
    - $1\text{nJ}/6\text{fJ} = 166,666$
Impact of Technology Scaling

ADC Resolution:

- 6bits
- 8bits
- 10bits
- 12bits
- 14bits
- 16bits

Energy Equivalent # of Gates

Feature Size [µm]
Observations

• Energy equivalent number of gates per A/D conversion has gone through the roof

• Reason
  – Digital circuits have scaled well with technology
  – Analog doesn't benefit quite as much from smaller features
    • Issues: Low supply voltage, low device gain, ...

• Key idea
  – Build "digitally assisted analog circuits"
  – Find a way to leverage digital processing capabilities to improve performance and lower power of analog circuits
Analog Circuit Challenges

Matching and linearity constraints are not fundamental
A New Generation of ADCs

• Conventional ADC
  – Precisely linear mapping from input to output
  – Relies on highly linear and well matched analog components

• Digitally assisted ADC
  – A "sloppy" one-to-one mapper
  – Digital postprocessor estimates ADC errors and applies corrections
Examples

- Digitally assisted pipeline ADC
  - Murmann & Boser, ISSCC 2003

- Minimum complexity, ultra low energy pipeline ADC
  - Under development in my research group

- ADC with embedded calibration for OFDM systems
  - Under development in my research group
Pipeline ADC

- Bottleneck: Highly linear gain element
Open-Loop Gain Element

Conventional Precision Amplifier

Open-Loop Amplifier

+ Lower Noise
+ Increased Signal Range
+ Lower Power
+ Faster

— Nonlinear

➢ Use DSP to linearize!
Digital Nonlinearity Correction

- Use digital system identification techniques to determine optimum post distortion function
- Possible (and often necessary) to track correction parameters without interrupting normal ADC operation
Experimental Verification

- 12bit, 75MSamples/sec, 0.35µm, post-processor off chip
- Based on commercial part (Analog Devices AD9235)
Block Diagram

- **Proof of concept design**
  - Open-loop amplifier only in first, most critical stage

- **Judicious analog/digital co-design**
  - Only two correction parameters (linear and cubic amplifier error)

~8400 Gates (0.042mm² in 0.13µm)
Linearity Improvement

![Graph showing linearity improvement with and without post-processing](image)
Amplifier Power

Commercial Part (Precision Amplifier)

This Work (Simple Amplifier)

-62% (33mW)
Digital Post-Processor

- 8400 Gates, 64 bytes RAM, 64kBit ROM
- Place & Route in 0.35\(\mu\)m technology

Area = 1.4 mm\(^2\) (18%)

Power = 10.5 mW (3.6%)

Pipelined ADC (7.9 mm\(^2\))
Going Beyond a Proof of Concept

- Proof-of-concept design showed that the idea of digital assistance works, but power savings were not "revolutionary"
- As a more aggressive step, it is now interesting to explore the question:

How many "analog" transistors do we really need?
Minimalistic Pipeline ADC Stage

- Use a single active device, operated like a charge pump to implement gain element
- Highly energy efficient, low noise, …
- Gain is imprecise and nonlinear, but post-processor can take care of that
Simulated Energy/Conversion

- 9-bit, "minimalistic" pipeline ADC prototype in 90nm technology
  - Roughly 20,000 gates used for digital post-processing
  - Only 7pJ per conversion, ~50x below state-of-the-art
Attributes (1)

- At 10M Samples/s (~video-rate), this ADC consumes only 70\(\mu\)W
- Can be powered from a 1cm\(^3\) size battery for more than 1 year!
  - A state-of the art ADC will drain the battery within a few days…
Attributes (2)

- Energy/conversion is dominated by digital post-processing
- Great news!
  - Energy efficiency will improve further when design is scaled to 65nm, 45nm, …
The Calibration Problem

• The "sloppier" we make the analog portion of the ADC, the more parameters we need to estimate and track
  – Can become quite complex or even impossible without disturbing normal ADC operation

• Idea: "System Embedded" postprocessing and calibration of ADC
  – Leverage redundancy and knowledge of certain input signal properties to estimate ADC errors
  – Re-use existing system resources for ADC calibration

• Example: ADC for OFDM receivers
Embedded ADC Calibration for OFDM

- Communications protocol uses "pilot tones" to measure and equalize RF channel nonidealities
- Why not use these pilots to "equalize" ADC?
  - Errors in pilot signals can be used to estimate correction parameters for sloppy ADC
Typical Learning Curve

SNDR (dB)

iteration

ENO=6 bits

~100ms
Conclusions (1)

• Analog circuit improvements lag progress of digital functions
  – Technology scaling only conditionally benefits analog circuit performance

•Digitally assisted analog circuits offload accuracy constraints to digital processor

• ADCs are obvious candidates for "digital assistance"
  – The benefits of digital pre/postprocessing are also being investigated for several other analog circuit blocks
    • Signal pre-distortion in RF power amplifiers
    • Signal pre-distortion in DACs
    • High-speed wireline interfaces
Conclusions (2)

• Key benefits
  – Lower power and potentially higher speed
    • Up to 100x reduction in ADC energy/conversion
  – Digitally assisted ADCs will benefit from future technology scaling
    • "Sloppy" circuits will be compatible with low voltage, low gain, ultimately scaled CMOS

• Key challenges
  – Interdisciplinary nature of design problem
    • Device modeling, circuit design
    • Math, signal processing algorithms
    • Inclusion of application layer
  – Design complexity and turnaround time