SH-MobileG1: A Single-Chip Application and Dual-mode Baseband Processor

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*: Currently with Renesas Technology
Outline

- Overview
- SH-MobileG1 Architecture
  - 3 CPU Configuration
  - Communication Architecture
  - Interrupt Control
  - System Control
  - Power Control and Leakage Current
- Summary
3G Multi-Media Cellular Phone System

- HPA: High Power Amplifier
- RFIC: Radio Frequency IC
- Baseband Processor
- Application Processor
- Multi-Media Accelerator

Previous System

New System Using G1

One Chip SH-MobileG1
A Sample of System Architecture using G1
Motivation for One Chip Integration

- Chip-set cost will be down
- Mount area will be decreased by sharing common peripherals
- Performance will be up by wide data throughput
- Dynamic power will be saved by low-load inter-domain signals
- Static power will be saved by leakage current shut-off for unused domain
Chip Overview

Die size
- 11.15mm x 11.15mm

Process
- 90nm LP
- 8M(7Cu+1Al)
- CMOS dual-Vth

Supply voltage
- 1.2V(internal), 1.8/2.5/3.3V(I/O)

# of TRs, gate, memory
- 181M TRs,
- 13.5M Gate
- 20.2 Mbit mem
AP-Realtime Domain Configuration

- **SHX2 runs on RT-OS**
  - 2-way superscalar up to 312MHz
  - 32KB-I$ and 32KB-D$
  - 512KB onchipRAM
- **Media IPs**
  - VPU encodes MPEG4 and H.264
  - VIO handles up to 5M pixel camera.
  - 3D graphic accelerator

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**Diagram Labels:**
- S2S: SHwy-SHwy bridge
- SBSC: SDR/DDR-SDRAM Controller
- LCDC: LCD Controller
- VIO: Camera I/F with Image-Processing Engine
- VPU: Video Processing Unit (MPEG-4 Accelerator)
- JPU: JPEG Codec Unit
- 3DG: 3D Graphics Accelerator
- INTC: Interrupt Controller
- MFI: Multi-Functional Interface
AP-System Domain Configuration

- ARM926EJ-S runs on general-purpose OS
  - Up to 208MHz
  - 32KB-I$ and 16KB-D$

- Peripherals
  - Sound handling
  - SDcard, IIC
  - Flash Control
  - USB
  - BB communication serial
Baseband Domain Configuration

- **ARM926EJ-S** runs on RT-OS
  - Up to 104MHz
  - 16KB-I$ and 4KB-D$ with TCM
- **W-CDMA and GSM/GPRS**
  - DSP accelerates the modem protocol handling
  - One can be cut-off where only the other is available
  - Only small logic is awake for tracing the timing of each radio
Communication Architecture

- G1 keeps the communication paths (MFI and Serials) used in the previous system for software reuse.
Communication Architecture (Cont’d)

- AP-SYS and AP-RT share SDRAM and memory map
- AP and BB have different SDRAM and memory map
- APBB bridge supports access window scheme to access the resource in the other memory map

<table>
<thead>
<tr>
<th>BB Address Map</th>
<th>AP Address Map</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flash</strong></td>
<td><strong>Flash</strong></td>
</tr>
<tr>
<td><strong>BB SDRAM</strong></td>
<td><strong>SYS Peripheral Regs</strong></td>
</tr>
<tr>
<td><strong>AP Access Window Using AP-BB bridge</strong></td>
<td><strong>AP SDRAM</strong></td>
</tr>
<tr>
<td><strong>BB Peripheral Regs</strong></td>
<td><strong>BB Access Window Using AP-BB bridge</strong></td>
</tr>
</tbody>
</table>

Map any region of AP address by register settings

Map any region of BB address by register settings
Interrupt Control

- Each CPU has its INT controller
- MFI can generate inter-domain interruptions
- Some external pins generate interrupts for each CPU
System Control

- **S**: Semaphore Register
- **P**: Power Down Register
- **W**: Wake-up Register
- **B**: Boot Control Register

**Diagram**:
- **Baseband CPU**
  - Reset Clock
  - Boot Address
- **AP-SYS CPU**
  - PLLs
  - Reset Clock
- **AP-RT CPU**
  - PLLs
  - Reset Clock

**Register List**:
- **SYSCBB**
- **SYSCSYS**
- **SYSCRT**

**Clocks**:
- **SYSC (Common)**
- **Semaphore Free: 00**
- **RT: 01**
- **SYS: 10**
- **BB: 11**

**Other Controls**:
- **Power Control**
- **Boot Control** (Master CPU, Boot Address for each CPU)

**Miscellaneous**:
- **RESET**
- **WakeUp**
System Control (Cont’d)

- **Boot Control**
  - One master CPU defined by pin settings boots first and specifies the other CPUs’ boot addresses
  - Various boot modes are supported for system configurability and debuggability

  1. BB Master External Memory Boot
  2. BB Master Internal ROM Boot
  3. BB-Alone Mode (for Test)
  4. AP-SYS Master External Memory Boot
  5. AP-SYS Master Internal ROM Boot
  6. AP-RT Master Boot
  7. AP-Alone Mode (for Test)
System Control (Cont’d)

- **Power Control**
  - Each CPU can read and write SYSC registers from each domain, which are reflected into the common SYSC
  - Power up/down can be controlled by each CPU that gets the semaphore

- **Clock Control**
  - AP and BB have separate Clock Pulse Generator
  - Many variations of clock configuration and gear changes are supported for dynamic power reduction
  - Clock for some IPs remains the fixed frequency
Power Domain

- 20 hierarchical domains for partial power-off

Application part

- C5 (System controller, PAD controller)

Baseband part

- C4 (Repeaters, CK buffers, BKUP FFs)

- Mem Control. RAM, DMA

PLL for Application part

- PLL for Baseband part

Mobile Video Interface

- Mem control. Serial I/Os

- SYS-CPU

- RT-CPU

- BB-CPU

- WCDMA

- GSM

- DFT

- WCDMA

- GSM

- BW1

- BW2

- BW3

- BA2

- BA3

- BA4

- BC

- BG1

- BG2

- BG3
Power Domain (Cont’d)

Chip Floorplan

- W-CDMA
- AP-Misc
- 3DG
- Camera
- APL-RT
- GSM
- AP-SYS
- CPU
- Media
- RAM

Power Domains

- GSM
- W-CDMA
- BB-Misc
- BB-CPU
- Media
- Sound
- 3DG
- MPEG
- JPEG

REFERENCES

- RE2B2
- BG1
- BG2
- BG3
- BA2
- BA3
- BA4
- A2
- A1R
- A1A
- A4U1
- A4U2
- A4U3
- A4U4
- C4
- C5
- BW1
- BW2
- BW3
- BC1
- AC
# Implementation Results of Power Domains

<table>
<thead>
<tr>
<th># of Power domains</th>
<th>20 domains</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Islands for C4</td>
<td>19 islands</td>
</tr>
<tr>
<td>(Repeaters, CK buffers, BKUP FFs)</td>
<td></td>
</tr>
<tr>
<td># of Repeaters in C4 domain</td>
<td>3100 cells</td>
</tr>
<tr>
<td># of Clock buffers in C4 domain</td>
<td>1600 cells</td>
</tr>
<tr>
<td># of Backup FFs in C4 domain</td>
<td>2300 cells</td>
</tr>
<tr>
<td># of mIOs (isolation cell)</td>
<td>20000 cells</td>
</tr>
<tr>
<td>Total area of power switch</td>
<td>4.2 mm²</td>
</tr>
</tbody>
</table>
Leakage Current in Usage Scenes

(1) Video telephony

<table>
<thead>
<tr>
<th></th>
<th>Baseband part</th>
<th>Application part</th>
<th>Measured Leakage Current (@ Room Temp, 1.2V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Control</td>
<td>System-domain</td>
<td>849 µA</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>ON / OFF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ON / OFF</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>ON</td>
<td></td>
</tr>
</tbody>
</table>
## Leakage Current in Usage Scenes

### (2) Telephony (W-CDMA)

<table>
<thead>
<tr>
<th></th>
<th>Control</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseband part</td>
<td>W-CDMA</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>GSM</td>
<td>ON / OFF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Application part</th>
<th>System-domain</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Realtime-domain</td>
<td>OFF</td>
</tr>
</tbody>
</table>

| Measured Leakage Current (@ Room Temp, 1.2V) | 407 $\mu$A |

### Diagram

- **Power on**
- **Power off**
Leakage Current in Usage Scenes

(3) Waiting for Calling

<table>
<thead>
<tr>
<th>Control</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>W-CDMA</td>
<td>OFF *</td>
</tr>
<tr>
<td>GSM</td>
<td>OFF</td>
</tr>
<tr>
<td>System-domain</td>
<td>OFF</td>
</tr>
<tr>
<td>Realtime-domain</td>
<td>OFF</td>
</tr>
<tr>
<td>Measured Leakage Current (@ Room Temp, 1.2V)</td>
<td>299 µA</td>
</tr>
</tbody>
</table>

*: Intermittent Operation
Leakage Current in Usage Scenes

(4) Power off (I/O fixed)

<table>
<thead>
<tr>
<th>Part</th>
<th>Control</th>
<th>W-CDMA</th>
<th>GSM</th>
<th>System-domain</th>
<th>Realtime-domain</th>
<th>Measured Leakage Current (@ Room Temp, 1.2V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseband part</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>7 µA</td>
</tr>
<tr>
<td>Application part</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
</tr>
</tbody>
</table>

Power on

Power off
Summary

- We have developed SH-MobileG1
  - Application and dual-baseband single-chip processor for 3G multimedia cellular phone system
  - Key features of its architecture have been presented
  - One chip integration contributes not only to dynamic but also to leakage current reduction by careful partial power-off control