Professional H.264/AVC CODEC Chip-set for High-quality HDTV Broadcast Infrastructure and High-end Flexible CODEC Systems

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Outline

- History of NTT’s Video CODEC Chips
- Background and Motivation
- What is HDTV Broadcast Infrastructure
- SARA Key Features and Functions
- SARA Main Architecture
- SARA Chip Implementation
- SARA High-end Flexible CODEC Systems
- Summary
History of NTT’s Video CODEC LSIs

ENC-C/-M (’95) (HotChips7)

SuperENC (’98) (HotChips10)

Encoder PC Card (ICCE2000)

Portable HDTV Encoder (ICCE2001) SuperENCx9

SDTV HDTV

HDTV Camera (NAB2001)

Encoder PCI Board (Globecom95)

ISIL-BOX (CoolChips2006)

SHR (NAB2004)

ISIL (’02) (CICC2003)

NHK/NTT-COM (News2002)

ISIL-II (’07) (CoolChips2007)

VASA (’02) (HotChips14)

Professional:
- DTV Service
- Super HD

Consumer/Prosumer:
- HDV Camera
- Video Phone

MPEG2 H.264

SARA* (’07) (HotChips19)

(*)SARA: Super Advanced Real-time CODEC Architecture for H.264 professional implementations

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Background and Motivation

- Global wave of H.264 technologies for high efficiency video coding of various HDTV applications.
  - Storage: BD, HD-DVD, AVCHD of optical disc and video camera for consumer.
  - Broadcasting: future digital broadcasts of several countries with Europe DVB-H, Japanese ISDB-T, and US-ATSC have been scheduled already.
  - Main carriers in the world, NTT also, have announced IP-based visual services, IPTV, VOD, and re-transmission of airwave, via IP-broadband network.

- Available chips are …
  - Domino[X], Ambarella, SONY, Fujitsu, … for consumer,
  - Telairity (processor-based) for professional (Hot Chips17) and so on.

- There are few chips with sufficient performance and flexibility for professional applications.

- **SARA**: Professional H.264/AVC CODEC Chip-set for HDTV Broadcast Infrastructure and High-end Flexible CODEC Systems.
What is HDTV Broadcast Infrastructure

Digital TV Broadcasting Network Service (NTT Communications)
-- HDTV Transmission network for terrestrial digital broadcasting in Japan --

NTT-Com

Local TV Station

Embedded VASA

HDTV CODEC

NTT Com

Contribution Transmission

Edge

HDTV CODEC

Various High-end CODEC Systems

NTT
Various High-end CODEC Systems

MPEG-2 VASA’s Application Examples in Japan

- Compactness
- Low-power
- High-quality

Distribution System

- Low-bitrate
- High-quality

Interruption System

- Low-delay
- High-bitrate
- High-quality

Contribution System

Tandem & Transcoder

Low-delay HDTV Encoder

Portable Microwave Link

NHK/NTT-COM

NTT/NEC
SARA Key Features and Functions

- **H.264 high-quality CODEC for professional applications**
  - Contribution: 4:2:2, CBR, low-delay and high-bitrate
  - Distribution: 4:2:0, CBR, low-bitrate (high-compression)
  - Storage: 4:2:2/4:2:0, VBR

- **Real-time {H.264:MPEG-2} transcoding using recoding information and/or external preprocessing information**

- **Wide range of coding-modes for efficient encoding and transcoding** (CABAC/CAVLC, weighted prediction, variation of multiple reference frames, etc)

- **Preprocessing of picture characteristics extraction**

- **High-precision adaptive hierarchical motion estimation with optimized H.264's mode decision**

- **Dynamic selective entropy coding (CABAC/CAVLC)**
H.264 Algorithms and their Mapping

- Current image
- Coder Control
- Intra Prediction
- Motion Compensation
- Motion Estimation
- Transform
- Q
- Entropy Coding
- Inv. Transform
- Inv.Q
- Loop Filter
- Reconstructed images

- Video Encoder Core
- RISCs
- IPD
- ME
- MC
- TQ
- EC
- LF

- Data Transfer
- Memory Interface

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SARA Architecture (Block Diagram)

Host Processor

Communication Data

TRISC

V-CORE

VRISC

SME

TME

FME

IPD

C-CORE

CRISC

EC

LF

TQ

From/to Upper chip

From/to Lower chip

Video Data

Audio/user Data

TS

From/toUpper chip

From/to Lower chip

Mobile DDR

eDRAM

Multiplication Core Encoding Scheme

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Photograph of SARA
# SARA Physical Features

<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of transistors</td>
<td>140 million transistors</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>200 MHz/ Max.</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>Core: 1.2 V / I/O: 3.3 V / eDRAM: 2.5 V / Mobile DDR 1.8 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.0 W/ Max.</td>
</tr>
<tr>
<td>Package</td>
<td>625-pin FCBGA (21mm x 21 mm)</td>
</tr>
<tr>
<td>External memories</td>
<td>512 Mbit (32 bit) Mobile-DDR</td>
</tr>
</tbody>
</table>
## SARA Function Features

<table>
<thead>
<tr>
<th>Video</th>
<th>Profile and level</th>
<th>Search range</th>
<th>Resolution and video rate</th>
<th>Transcoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Profile: H.264 Main / High / High422(8bit only)</td>
<td>-217.75/+199.75(H), -109.75/+145.75(V)</td>
<td>Encoding: Single-chip: 720 x 480 at up to 30 frames per second</td>
<td>Combination of H.264/MPEG-2 input and H.264/MPEG-2 output using recoding and/or our original information</td>
</tr>
<tr>
<td></td>
<td>Level: 3.0 / 4.0 / 4.1</td>
<td></td>
<td>Multi-chip: 1920 x 1080 at up to 30 frames per second</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MPEG-2 {MP, 422P} @ {ML, HL}</td>
<td></td>
<td>Decoding: 720 x 480 at up to 30 frames per second</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1920 x 1080 at up to 30 frames per second</td>
<td></td>
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<tr>
<td>Pre-processing</td>
<td>Macroblock based functional filters</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Macroblock based feature extraction functions</td>
<td></td>
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<tr>
<td>Audio</td>
<td>I/O Format</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Linear PCM or Encoded stream (AAC)</td>
<td></td>
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<tr>
<td></td>
<td>Handling by external audio codec</td>
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<tr>
<td>User</td>
<td>I/O Format</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>PES format for timecode and another audio data</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System</td>
<td>I/O Format and Bitrate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MPEG-2 TS(188/204 bytes) Max. 120 Mbps</td>
<td></td>
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</tr>
</tbody>
</table>
SARA Multi-chip HDTV Module

Very Compact Post-card-size HDTV Module with transcoding capability
SARA Evaluation and Validation

Before fabrication,
HW/SW were carefully evaluated and validated using VCS and ASIC emulator through small- and/or full-size images.

After fabrication,
HW/SW were evaluated and validated using SARA CODEC evaluation boards.

The first silicon is successfully implemented with complete software.
High-end Flexible CODEC Systems

- Very compact post-card-size HDTV modules with transcoding capability.
- Building-block based flexible CODEC systems for various professional applications,
  - MPEG-2/H.264 real-time transcoder for IP based H.264 re-transmission from radio wave broadcasting (MPEG-2),
  - H.264/H.264 real-time transcoder for future complete H.264-based digital TV broadcasting,
  - H.264-based tandem (two-passed) encoding for higher-compression (lower-bitrate) of final distribution.

SARA Modules

Module-IF With FPGA

Module-IF with FPGA(ENC/DEC)

CODEC Board IF

Several CODEC Combinations
SARA Flexible CODEC System (1/2)

SARA H.264
(Encoder Module)

SARA High-Quality Encoder System
SARA Flexible CODEC System (2/2)

VASA MPEG-2
(Decoder Module)

SARA H.264
(Encoder Module)

SARA MPEG-2/H.264 Transcoder System
Summary

- Background and Motivation
- HDTV Broadcast Infrastructure
- SARA Main Architecture
  - H.264 Algorithms and their Mapping
  - Block Diagram and its MB Pipelined Scheme
- SARA Implementation
  - Physical & Functional Features
- SARA High-end Flexible CODEC System
  - High-quality Encoder System
  - MPEG-2/H.264 Transcoder System

**SARA** is a **key LSI** for implementing various professional H.264/MPEG-2 applications for future broadcast infrastructure.