System Architecture and Applications of the PNX5100
A high-performance full HD 120p Hz post-processing engine

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Outline

- Introduction: Video Processing in high-end TV
  - Why Frame Rate Conversion
  - Picture Quality, Market Requirements
  - The PNX5100 (system, SoC, Video sub-system)

- Highlighted Features
  - High Definition Halo Reduced Frame Rate Conversion
  - The TM3271 media processor
  - On the fly compression of video traffic from/to SDRAM memory

- PNX5100 product status

- Lessons learned / Outlook towards future
Introduction
Market outlook & value proposition
Frame Rate Conversion

- **Why (Source): Movie Judder Cancellation**
  - Movie content is shot in 24 Hz and displayed traditionally at 60 Hz. This is achieved by alternating repeating original pictures 3 and 2 times, called 3:2 pulldown
  - Visually 3:2 pull-down leads to Motion Judder which is especially noticeable on larger display
  - Movie Judder can be removed by means of applying Motion Compensated Frame Rate Conversion (Movie Judder Cancellation)

- **Why (Display: LCD): Motion Blur Reduction**
  - LCD displays are so called sample-and-hold displays (pixel values are frozen for the duration of the frame)
  - Visually, the sample and hold effect leads to Motion Blur (images seem less sharp once they start moving)
  - Effect can be reduced by displaying at higher frame-rates (120 Hz) and apply Motion Compensated Frame Rate Conversion

- **Bottom line**
  - Frame Rate Conversion is key to remove movie-judder-cancellation and motion-blur-reduction

- **How**
  - 2 frame block based Motion Estimation + Motion Compensated Temporal Up-conversion
  - 3 frame block based Motion Estimation + Motion Compensated Temporal Up-conversion with occlusion detection
Picture Quality Leadership

- NXP has a long pedigree of World class Picture Quality products

- We are the inventors of Frame Rate Conversion
  - High Definition: PNX5050 (2007),
  - Full HD Halo Reduced: PNX5100 (2008), PNX85500 (2009)
  - NXP has extended patent portfolio
    - Exclusive ownership of Frame Rate Conversion (ME/MC) patent family; traditional as well as Halo Reduced

- NXP has advanced LED Backlighting technology
  - 2D Luminance and Color Dimming/boosting
  - Strong patent portfolio

- Extended NXP Innovation in color / spectrum sequential BL technologies
Hybrid TV system

Complete one chip TV:
- Cost sensitive midrange market
- Connectivity, OSD
- Hybrid source decode
- De-interlacing
- Audio/Video processing

Picture Quality processor
- Halo reduced HD Frame Rate Conversion
- LCD Motion Blur Reduction
- Display color and Contrast enhancements

1920x1080p @120hz
PNX5100
SoC view

- **Computing system:**
  - 3 x TM3271 32I/64D

- **Video processing & rendering:**
  - CPIPE, 2 video layers, 1 GFX layer
  - UIP Format conversion and measurement

- **Memory interface:**
  - DDR-2 667 MHz 32-bit interface

- **External Video input:**
  - 2 x LVDS Rx
  - Up to 1920x1080p 60hz
  - (including 1/9 display res. PIP in H/V blanking)
  - Additional digital ITU601 input for sub-channel video data

- **External Video output:**
  - 2x or 4x LVDS Tx
  - Up to 1920x1080p 60hz / 1366x768p 120Hz
  - Up to 1920x1080p 120 Hz
  - Vector & Depth info for 3D support in VBI

- **Peripherals:**
  - PCI
  - (Boot, GFX transfer, Debug)
  - 2x I2C (I2C → DMA)
  - EJTAG
  - UART/GPIO’s
  - GPIO (16, 4 PWM)
Layout view of PNX5100

Process:
CMOS090 LP (7 Layers)
Number of Pads: 674

Package:
456 BGA
35 mm body
1.27 mm pitch
4 layer BGA substrate
Core power 4.5 Watt

U1: TM3271 x 3, PCI, I2C, etc.
U2: LVDS Tx,
U3: CPIPE (Video output)
U4: LVDS Rx, UIP (Video Input)
U5: Clocks
U6: DDR2, DMA Controllers
Video Sub-system
Block Diagram

Motion Estimation
Vector Processing
Film mode detection

Frame Rate Conversion

Temporal Up-conversion to 120 Hz
Static Region Detection

Advanced Video Features
PiP
OSD/GFX

SoC Control
Auto Picture Control
Video Sub-system

Highlighted Features

1. High Definition Halo Reduced Frame Rate Conversion

2. The TM3271 Media processor

3. On the fly compression of video traffic from/to SDRAM memory

- Above are discussed further in remainder of presentation
High Definition Halo Reduced Frame Rate Conversion
Frame Rate Conversion

2-frame Motion Estimation

- Find a matching block between current and previous picture
- Problem in occlusion area (left side of the helicopter)
Frame Rate Conversion

Up-conversion

- Motion Compensated Temporal interpolation uses the motion vectors from the Motion Estimator

  Halo artifact clearly visible

- Wrong vector in occlusion area causes an artifact called ‘Halo’

- Occlusion issue cannot be resolved as insufficient data is available
Frame Rate Conversion
3-frame Motion Estimation

- Find a matching block in next AND/OR previous image
- Occlusion problem solved
- A match can be found in either the previous or the next image
Frame Rate Conversion

Results for 3 and 2-frame motion estimation

- Halo largely gone
- Halo clearly visible

With Halo Reduction

Without Halo Reduction
Frame Rate Conversion
Effectively deploying programmability

- Only part of the image needs a complex up-conversion algorithm
- Programmable platform can handle different algorithms for different parts of the image very efficiently

<table>
<thead>
<tr>
<th>Temporal Up-conversion Algorithm</th>
<th>Computational Complexity</th>
<th>Percentage of blocks (avg, max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consistent</td>
<td>Low</td>
<td>60%, 80%</td>
</tr>
<tr>
<td>Inconsistent</td>
<td>High</td>
<td>30%, 40%</td>
</tr>
<tr>
<td>Occlusion</td>
<td>High</td>
<td>6%, 10%</td>
</tr>
<tr>
<td>Static / Border</td>
<td>Medium</td>
<td>4%, 10%</td>
</tr>
</tbody>
</table>

**Temporal Up-conversion**

- **Video input**
  - Consistent
  - Inconsistent
  - Static region
  - Border
  - Occlusion

- **Video output**

**worst case 50% high complexity**
The TriMedia3271 Media processor
Computing Engine

TM3271 Main Characteristics

- Fully synthesizable design (450/350 MHz)
- VLIW machine with 5 issue slots
- 32-bit address range, 32-bit datapath
- 32 Kbyte instruction cache (8-way set associative)
- 64 Kbyte data cache (4-way set associative)
- Operations are guarded
- Unified 128x32-bit register-file
- 35 execution units
- Application specific operations
- SIMD multimedia and IEEE754 FP operation support
- Variable length instruction encoding
- Pipeline depth 7-12 stages

TM3270 discussed at Hotchip18 in “Home entertainment-quality multimedia experience whilst on the move”
Computing Engine
Performance of FRC on TM3271

- Motion Estimation:
  - 3DRS: 150 Mcycles/s
    - Block Matching between 3 pictures
    - 8 candidates per block
    - Sub-pixel processing
  - Motion Vector Processing: 60 Mcycles/s

- Halo Reduced Motion Compensated Temporal Up-conversion:
  - Pixel Interpolation: 330 Mcycles/s
  - Measurements: 110 Mcycles/s

- Cadence Detection:
  - Universal Cadence Detection 30 Mcycles/s

- Total: 680 Mcycles/s

- Internal benchmark data:
  - General purpose CPU’s: 10-50 GHz required
On-the-fly compression of video traffic from/to SDRAM memory

Video Compression
Video Compression (VC)
Context and Objectives

- **Context:**
  - Memory Bandwidth is a Bottleneck in High performance image processing SoCs.
  - Achieve reduction in Memory Bandwidth by using Embedded Video Compression
  - Compress the Video Data before writing to Memory and uncompress the data while reading from Memory
  - Consists of Encoder and Decoder

- **Objectives**
  - Visually lossless picture quality
  - Reduction of SDRAM bandwidth
  - Limited/acceptable impact on SDRAM latency

- **Video Compression was considered to reduce the memory interface speed risk**
  - In final product, compression is not enabled as the use-case requirements can be met without compression
Video Compression

Algorithm

- Based on DPCM and Variable Length Coding
- Process packets of 128 data samples
- Remove LSBs until compressed size fits the specified output size
- **Visually lossless** up to ratio 1.6 – 2.0, depending on content
Video Compression for PNX5100

- **Rationale:**
  - Enable lower frequency DDR-2
  - Low development risk
  - Large BW savings achievable

- **Formats supported**
  - YUV422
  - 8 or 10 bit video

- **Compression factor**
  - From 1.2 to 3

- **Latency / Throughput**
  - 80 cycles for Encoder (128-byte input)
  - 60 cycles for Decoder (128-byte input)
  - 1 pixel / cycles (300 Mpixel/s)

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<table>
<thead>
<tr>
<th>BW in Mbyte/s and relative needed BW</th>
<th>Total gross BW without Video Compression</th>
<th>Total gross Bandwidth with Video Compression of 1.8</th>
<th>Relative BW savings</th>
</tr>
</thead>
<tbody>
<tr>
<td>1920x1080x120p, 333 MHz DDR-2</td>
<td>2047 (81%)</td>
<td>1771 (70%)</td>
<td>11%</td>
</tr>
<tr>
<td>1920x1080x120p, 300 MHz DDR-2</td>
<td>2047 (89%)</td>
<td>1771 (77%)</td>
<td>12%</td>
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</table>
PNX5100 Status / Summary / Lessons learned / Future outlook
Status PNX5100

- Silicon first time right!
- SW pre-development on Emulator and FPGA was enabler to have a demonstrator ready 2 weeks after samples arrived.
- PNX5100 and its application was successfully demonstrated at IFA2007 and CES2008
- Mass production has started with many customers, e.g.:
  - Panasonic, Philips, Loewe, Vestel, TCL, B&O, Vizio
- Excellent market feedback on picture quality, e.g.:
  
  Roland Bohl, director for R&D at Loewe said: “As the HD LCD TV market matures and consumers demand progressive improvements in their viewing experience, the ability to up-convert and deliver life-like picture quality will be a key differentiator for Loewe. Having evaluated a number of video processors on the market, we found NXP to offer the right platform for up-conversion to realize our philosophy of image enhancement (Image+ HD 100) in order to complement Loewe's premium LCD TV strategy - stylish design with superior picture quality.”

- European Imaging and Sound Association (Eisa) Award to be announced late August 2008
Lessons Learned / Summary / Future Outlook

- Major design challenge
  - Communication to SDRAM; rather than computation
  - Memory bandwidth predictability as a design constraint

- Flexibility through programmability
  - Innovation of FRC algorithms continue in parallel of SoC development
  - Problem solving more optimal

- Continuing need for increased performance
  - Quad full HD resolution (4 x compared to 1920x1080)
  - 240 Hz frame-rates (2 x compared to 120 Hz)
  - Pixel resolution (from 10 to 12 to 16 bit)
  - Further innovation on Picture Quality of FRC function (2 x)

- NXP new development: PNX85500
  - Further improvement of FRC function
  - Cost down of function
  - Integration in front-end/TV IC