Virtex-5 FXT
A new FPGA Platform, plus a Look into the Future

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FPGA Evolution

• **Moore’s Law:** Double density every other year
  New process technology, smaller geometry and always a new FPGA family
• **Traditionally:** bigger + faster + cheaper = better
• **Now:** more functionality, more hard cores, lower cost per function, better software
• **But:** raw speed does not come for free anymore, and leakage current is our worst enemy
Virtex-5

“The Gods Were Smiling…”

- The **process** was available early, and yields well
- **Features** were aggressive, but well-defined
- **Circuit design** was solid
- **Testing** was well-planned and executed
- Rapid introduction of **5 sub-families** (Platforms)
  - ‘LX, ‘LXT, ‘SXT, ‘FXT and ‘TXT (26 devices total)
- There was (and still is) **no real competition**
  > 90% share of market (>$50 M in first half of 2008)

**18 different devices in volume production now**
Virtex-5 Common Features

- 6-LUT + Express Fabric
- 36Kb Dual-Port Block RAM / FIFO with ECC
- SelectIO with IDELAY/ODELAY and SerDes
- GTX 3.75 Gbps Transceivers
- GTP 6.5 Gbps Transceivers
- PCI-Express Endpoint Blocks
- 10/100/1000 Mbps Ethernet MAC
- PowerPC440 Processors
- 550 MHz Clock Management
- 25x18 DSP Slices
- Integrated System Monitor A/D Converter
- Advanced Configuration Options

- 30% Higher Performance
- Higher Bandwidth
- Higher Precision
- New Capability
- Precision + low jitter
- Saves Logic
- New Capability
Virtex-5 FXT
Additional Capabilities

• One or two PPC440 hard Microprocessor cores faster and more efficient than PPC405, super-scalar, larger caches, deeper instruction pipeline, integrated crossbar switch saves thousands of slices

• GTX High-performance Transceivers optimized for performance and low power and pc-board signal integrity for an “open eye”.

5 family members, 3 in volume production by Sept.08
More Than Just a PPC440...

- **5 x 2 Crossbar Connection (128-bit interfaces)**
  - Reduces need for external buses
  - Allows **two operations** simultaneously

- **Memory Controller Interface**
  - Reduces latency and logic

- **Four 32-bit DMA Channels**

- **Auxiliary Processing-Unit Controller**
  - to attach soft co-processors
  - 128 bit interface, supports pipelining
Crossbar in Action

- Four built-in DMA channels provide high speed access to memory or I/O
- Separate memory and I/O buses greatly improve system performance
- External masters can access memory or I/O through the crossbar
Auxiliary Processor Unit Control

• Reduces PPC/APU overhead and increases data throughput

• Access to soft execution units e.g. Floating Point Coprocessor
  – Adds 16 user-defined instructions
  – 128-bit load/store interfaces
  – Pipelines instructions
  – Buffers data for up to 3 instructions

Tight coupling between CPU and soft logic cores
128-bit Floating Point Unit

- Soft co-processor module, free-of-charge accessible by the 440 processor instruction pipeline
- Single- and double-precision IEEE-754 compliant
- Speed-up 6 to 30 times, 200 MFLOPS sustained
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Low-Power Transceivers

- Gen 1
  - Tx Pre-emphasis
  - SONET Path
  - PCI-Express

- Gen 2
  - Advanced Rx EQ
  - Low latency
  - Low Power
  - PCI Express IP
  - Virtex-5
    - GTX
      - Advanced Rx EQ
      - Low latency
      - Low Power
      - PCI Express IP
  - GTP
    - Low Power
    - PCI-Express PHY
    - PCI Express IP
    - Easy to Use

- Gen 3
GTX Multi-Gigabit Transceiver

- 8 to 24 transceivers per device (40 and 48 in ‘TXT subfamily)
- Supporting data rates from 150 Mbps to 6.5 Gbps
- Power dissipation less than 250 mW per channel
- Programmable Tx pre-emphasis and Rx equalization
• Programmable Tx swing (diff): 1.3V, 1.2V, 1.1V, 1.0V, 900, 800, 700, 500mV
• Tx pre-emphasis*: 0%, 8%, 17%, 25%, 33%, 42%, 50%, 58% (nominally)
• Maximum peak-to-peak jitter: 0.32 UI @ 6.5 Gbps (~50ps) see Characterization Report
• Serial and Parallel loop-back capability for testing
• Out of Band (OOB) signal generation

* Also referred to as “de-emphasis”
• 4 modes of **analog** receive equalization **plus** Decision Feedback Equalizer (DFE)
• Programmable receive termination; supporting PCIe and SATA
• Can track +0 / -0.5% spread-spectrum clock at 30-60 kHz rate
• Receiver eye-scan capability for testing
• Ability to turn off Clock-Data Recovery tracking and to control CDR phase offset
Multi-Tap Digital Equalizer

First three taps have the biggest impact
**GTX: Additional Features**

- Handles 150 consecutive 1’s or 0’s without losing lock
- 8B/10B, 64B/66B, and 64B/66B Interlaken supported with “Gearbox”
- Built-in Burst-Error Test support
  - Pseudo Random Bit Sequence generator/checker: PRBS $2^7$, $2^{23}$, $2^{31}$
- Deterministic through-delay option with low latency
  - Bypasses encoders and FIFOs

*All GTX Transceivers have the same specifications and have full functionality*
6.5 Gb/s Transmit Eye Opening

Always keep your eyes open...
From Our Public Characterization Report...

http://www.xilinx.com/support/documentation/virtex-5.htm#19312
New Additions to the Family

- XC5VTX150T and ‘TX240T
- Like ‘FX130T and ‘FX200T minus the PPC microprocessor, but with **twice the number of GTX transceivers** 40 and 48 GTXs respectively
- Availability: ES 4Q08, Production 1Q09

*When you need lots of fast transceivers*
Moore's Law continues
2009 - 2013
Moore’s Law Continues

• 40/45 nm …… 32 nm …… 22 nm …… ?
  – Each step doubles density and thus max capacity
  – Each step lowers the cost per function
• But:
• More complex and more expensive masks
• Harder to control leakage current
• Larger parametric spread due to smaller feature size
• IC logic density outstrips pc-board pin-count
  – >6000 bumps on the flip-chip die, <1800 package pins
  – Stacked die to the rescue?

Progress gets harder and more expensive
Higher Speed is a Challenge

- Raw transistor speed is difficult to improve,
  - Supply voltage scaling reaches its limits.
- Performance is limited by the power & heat budget.
- Need for multiple technologies, optimized for either performance or power, not for both simultaneously.
- Multi-gigabit transceivers:
  - Conflict between highest bit-rate vs. widest frequency range (R-C vs. L-C type of VCO)

Higher speed does not come for free...
Users’ Design Productivity

• 10 x growth in FPGA capacity may challenge our users’ budget for design-time and cost.
• Design verification is biggest burden
• Design re-use becomes more important. More cores.
• Incremental compile and block-based design.
  – Place-and-route times must stay acceptable.

How to manage mega-gate designs at reasonable cost
Summary

- Virtex-5 is the winner, without any real competition
  - Xilinx strategy of sub-families proved to be very successful
- Multi-gigabit transceivers are very popular
- Moore’s Law will give us much more logic and lower cost
  - Speed and power consumption pose a difficult challenge
- Users want and need to improve design productivity
  - The pace is becoming faster and more competitive.

*Xilinx will keep bringing you better chips and tools*

*Thank You!*