OpenCL*, Heterogeneous Computing, and the CPU

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Agenda

• Heterogeneous computing in OpenCL
  • Data parallelism in OpenCL
  • Task parallelism in OpenCL
  • Future direction for parallel computing
Heterogeneous computing

• A modern platform has:
  – Multi-core CPU(s)
  – A GPU
  – DSP processors
  – ... other?

• The goal should NOT be to “off-load” the CPU. We need to make the best use of all the available resources from within a single program:
  – One program that runs well (i.e. reasonably close to “hand-tuned” performance) on a heterogeneous mixture of processors.

GMCH = graphics memory control hub,  ICH = Input/ output control hub
OpenCL: it’s not just a GPGPU Language

- OpenCL defines a platform API to coordinate heterogeneous parallel computations
  - Literature rich with parallel coordination languages/API
  - OpenCL unique in its ability to coordinate CPUs, GPUs, etc

- Key coordination concepts
  - Each device has its own asynchronous workqueue
  - Synchronize between OCL computations w/event handles from different (or same) devices
  - Enables algorithms and systems that use all available computational resources
  - Enqueue “native functions” for integration with C/C++ code
Agenda

- Heterogeneous computing in OpenCL
- **Data parallelism in OpenCL**
- Task parallelism in OpenCL
- Future direction for parallel computing
OpenCL’s Two Styles of Data-Parallelism

- Explicit SIMD data parallelism:
  - The kernel defines one stream of instructions
  - Parallelism from using wide vector types
  - Size vector types to match native HW width
  - Combine with task parallelism to exploit multiple cores

- Implicit SIMD data parallelism (i.e. shader-style):
  - Write the kernel as a “scalar program”
  - Use vector data types sized naturally to the algorithm
  - Kernel automatically mapped to SIMD-compute-resources and cores by the compiler/runtime/hardware.

Both approaches are viable CPU options
Data-Parallelism: options on IA processors

• Explicit SIMD data parallelism
  – Programmer chooses vector data type (width)
  – Compiler hints using attributes
    – vec_type_hint(typlen)

• Implicit SIMD Data parallel
  – Map onto CPUs, GPUs, Larrabee, ...
    – SSE/AVX/LRBni: 4/8/16 workitems in parallel

• Hybrid use of the two methods
  – AVX: can run two 4-wide workitems in parallel
  – LRBni: can run four 4-wide workitems in parallel
Explicit SIMD data parallelism

- OpenCL as a portable interface to vector instruction sets
  - Block loops and pack data into vector types (float4, ushort16, etc).
  - Replace scalar ops in loops with blocked loops and vector ops.
  - Unroll loops, optimize indexing to match machine vector width

```c
float a[N], b[N], c[N];
for (i=0; i<N; i++)
    c[i] = a[i]*b[i];

<<< the above becomes >>>>
float4 a[N/4], b[N/4], c[N/4];
for (i=0; i<N/4; i++)
    c[i] = a[i]*b[i];
```

Explicit SIMD data parallelism means you tune your code to the vector width and other properties of the compute device
Explicit SIMD data parallelism: Case Study

- Video contrast/color optimization kernel on a dual core CPU

<table>
<thead>
<tr>
<th>Successive improvement</th>
<th>Hand-tuned SSE + Multithreading</th>
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</thead>
<tbody>
<tr>
<td>5%</td>
<td>Unroll loops</td>
</tr>
<tr>
<td>23%</td>
<td>Optimize vector indexing</td>
</tr>
<tr>
<td>186%</td>
<td>Vectorize (block loops, pack into ushort8 and ushort16)</td>
</tr>
<tr>
<td>40%</td>
<td>1 work-item per core + loops</td>
</tr>
<tr>
<td>20%</td>
<td>% peak performance</td>
</tr>
<tr>
<td>100%</td>
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Good news: OpenCL code 95% of hand-tuned SSE/MT perf.

Bad news: New platform, redo all those optimizations.
Towards “Portable” Performance

- The following C code is an example of a Bilateral 1D filter:

```c
void P4_Bilateral9 (int start, int end, float v)
{
    int i, j, k;
    float w[4], a[4], p[4];
    float inv_of_2v = -0.5 / v;
    for (i = start; i < end; i++) {
        float wt[4] = { 1.0f, 1.0f, 1.0f, 1.0f }; 
        for (k = 0; k < 4; k++)
            a[k] = image[i][k];
        for (j = 1; j <= 4; j++) {
            for (k = 0; k < 4; k++)
                p[k] = image[i - j*SIZE][k] - image[i][k];
            for (k = 0; k < 4; k++)
                w[k] = exp (p[k] * p[k] * inv_of_2v);
            for (k = 0; k < 4; k++)
                a[k] += w[k] * image[i - j*SIZE][k];
            wt[k] += w[k];
        } 
        for (j = 1; j <= 4; j++) {
            for (k = 0; k < 4; k++)
                p[k] = image[i + j*SIZE][k] - image[i][k];
            for (k = 0; k < 4; k++)
                w[k] = exp (p[k] * p[k] * inv_of_2v);
            for (k = 0; k < 4; k++)
                a[k] += w[k] * image[i + j*SIZE][k];
            wt[k] += w[k];
        } 
        for (k = 0; k < 4; k++)
            image2[i][k] = a[k] / wt[k];
    }
}
```

- Reminder: Bilateral filter is an edge preserving image processing algorithm.

- See more information here:
  [http://scien.stanford.edu/class/psych221/projects/06/imagescaling/bilati.html](http://scien.stanford.edu/class/psych221/projects/06/imagescaling/bilati.html)
Towards “Portable” Performance

- The following C code is an example of a Bilateral 1D filter:

- Reminder: Bilateral filter is an edge preserving image processing algorithm.

- See more information here: http://scien.stanford.edu/class/psych221/projects/06/imagscaling/bilateral.html

```c
void P4_Bilateral9 (int start, int end, float v) {

    <<< Declarations >>>
    for (i = start; i < end; i++) {
        for (j = 1; j <= 4; j++) {
            <<< a series of short loops >>>>
        }
        for (j = 1; j <= 4; j++) {
            <<< a 2nd series of short loops >>>>
        }
    }
}
```
**Implicit SIMD** data parallel code

- “outer” loop replaced by work-items running over an NDRange index set

- NDRange 4* image size ... since each workitem does a color for each pixel

- Leave it to the compiler to map work-items onto lanes of the vector units ...

```c
__kernel void P4_Bilateral9 (__global float* inImage, __global float* outImage, float v) {
    const size_t myID = get_global_id(0);
    const float inv_of_2v = -0.5f / v;
    const size_t myRow = myID / IMAGE_WIDTH;
    size_t maxDistance = min(DISTANCE, myRow);
    maxDistance = min(maxDistance, IMAGE_HEIGHT - myRow);
    float currentPixel, neighborPixel, newPixel;
    float diff;
    float accumulatedWeights, currentWeights;
    newPixel = currentPixel = inImage[myID];
    accumulatedWeights = 1.0f;
    for (size_t dist = 1; dist <= maxDistance; ++dist) {
        neighborPixel = inImage[myID + dist * IMAGE_WIDTH];
        diff = neighborPixel - currentPixel;
        currentWeights = exp(diff * diff * inv_of_2v);
        accumulatedWeights += currentWeights;
        newPixel += neighborPixel * currentWeights;
        neighborPixel = inImage[myID - dist * IMAGE_WIDTH];
        diff = neighborPixel - currentPixel;
        currentWeights = exp(diff * diff * inv_of_2v);
        accumulatedWeights += currentWeights;
        newPixel += neighborPixel * currentWeights;
    }
    outImage[myID] = newPixel / accumulatedWeights;
}
```
“Implicit SIMD” data parallel code

```c
__kernel void P4_Bilateral9 (__global float* inImage, __global float* outImage, float v)
{
    const size_t myID = get_global_id(0);
    const float inv_of_2v = -0.5f / v;
    const size_t myRow = myID / IMAGE_WIDTH;
    size_t maxDistance = min(DISTANCE, myRow);
    maxDistance = min(maxDistance, IMAGE_HEIGHT - myRow);
    float currentPixel, neighborPixel, newPixel;
    float diff;
    float accumulatedWeights, currentWeights;
    newPixel = currentPixel = inImage[myID];
    accumulatedWeights = 1.0f;
    for (size_t dist = 1; dist <= maxDistance; ++dist)
    {
        neighborPixel = inImage[myID + dist * IMAGE_WIDTH];
        diff = neighborPixel - currentPixel;
        currentWeights = exp(diff * diff * inv_of_2v);
        accumulatedWeights += currentWeights;
        newPixel += neighborPixel * currentWeights;
        neighborPixel = inImage[myID - dist * IMAGE_WIDTH];
        diff = neighborPixel - currentPixel;
        currentWeights = exp(diff * diff * inv_of_2v);
        accumulatedWeights += currentWeights;
        newPixel += neighborPixel * currentWeights;
    }
    outImage[myID] = newPixel / accumulatedWeights;
}
```

```
__kernel void p4_bilateral9(__global float* inImage, __global float* outImage, float v)
{
    const size_t myID = get_global_id(0);
    << declarations >>
    for (size_t dist = 1; dist <= maxDistance; ++dist){
        neighborPixel = inImage[myID + dist * IMAGE_WIDTH];
        diff = neighborPixel - currentPixel;
        currentWeights = exp(diff * diff * inv_of_2v);
        << plus others to compute pixels, weights, etc >>
        accumulatedWeights += currentWeights;
    }
    outImage[myID] = newPixel / accumulatedWeights;
}
```
Portable Performance in OpenCL

• Implicit SIMD code ... where the framework maps work-items onto the “lanes of the vector unit” ... creates the opportunity for portable code that performs well on full range of OpenCL compute devices

• Requires mature OpenCL technology that “knows” how to do this:
  – ...But it is important to note ... we know this approach works since its based on the way shader compilers work today
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Task Parallelism Overview

• Think of a task as an asynchronous function call
  – “Do X at some point in the future”
  – Optionally “… after Y is done”
  – Light weight, often in user space

• Strengths
  – Copes well with heterogeneous workloads
  – Doesn’t require 1000’s of strands
  – Scales well with core count

• Limitations
  – No automatic support for latency hiding
  – Must explicitly write SIMD code

A natural fit to multi-core CPUs
Task Parallelism in OpenCL

- `clEnqueueTask`
  - Imagine “sea of different tasks” executing concurrently
  - A task “owns the core” (i.e., a workgroup size of 1)

- Use tasks when algorithm...
  - Benefits from large amount of local/private memory
  - Has predictable global memory accesses
  - Can be programmed using explicit vector style
  - “Just doesn’t have 1000’s of identical things to do”

- Use data-parallel kernels when algorithm...
  - Does not benefit from large amounts of local/private memory
  - Has unpredictable global memory accesses
  - Needs to apply same operation across large number of data elements
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Future Parallel Programming

• Real world applications contain data parallel parts as well as serial/sequential parts

• OpenCL addresses these Apps need by supporting Data Parallel & Task Parallel

• Braided Parallelism – composing Data Parallel & Task Parallel constructs in a single algorithm

• CPUs are ideal for Braided Parallelism
Future parallel programming: Larrabee

- Cores communicate on a wide ring bus
  - Fast access to memory and fixed function blocks
  - Fast access for cache coherency
- L2 cache is partitioned among the cores
  - Provides high aggregate bandwidth
  - Allows data replication & sharing
Processor Core Block Diagram

- Separate scalar and vector units with separate registers
- Vector unit: 16 32-bit ops/clock
- In-order instruction execution
- Short execution pipelines
- Fast access from L1 cache
- Direct connection to each core’s subset of the L2 cache
- Prefetch instructions load L1 and L2 caches
Key Differences from Typical GPUs

• Each Larrabee core is a complete Intel processor
  – Context switching & pre-emptive multi-tasking
  – Virtual memory and page swapping, even in texture logic
  – Fully coherent caches at all levels of the hierarchy

• Efficient inter-block communication
  – Ring bus for full inter-processor communication
  – Low latency high bandwidth L1 and L2 caches
  – Fast synchronization between cores and caches

Larrabee is perfect for the braided parallelism in future applications
Conclusion

- OpenCL defines a platform-API/framework for heterogeneous computing ... not just GPGPU or CPU-offload programming

- OpenCL has the potential to deliver portably performant code; but only if its used correctly:
  - Implicit SIMD data parallel code has the best chance of mapping onto a diverse range of hardware ... once OpenCL implementation quality catches up with mature shader languages

- The future is clear:
  - Braided parallelism mixing task parallel and data parallel code in a single program ... balancing the load among ALL OF the platform’s resources
  - OpenCL can handle this ... and emerging platforms such as Larrabee are well suited to support this model
References

- **s09.idav.ucdavis.edu** for slides from a Siggraph 2009 course titled “Beyond Programmable Shading”


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