PNX85500 Single Chip LCD TV System
with integrated 120Hz HD Frame Rate Converter

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PNX85500 Single Chip LCD TV System
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Presentation Outline

- Introduction
- System Integration
  - More TV System on a Chip
  - PNX85500 TV Solution
- Design Challenges
  - Architecture
  - Memory Bandwidth and Latency
  - Verification and Emulation
- High-lighted Features
- Conclusions
Introducing the TV550 System

TV550 System comprises the world’s first Digital TV SoC in C045: PNX85500

- Extremely high level of functional integration
  - Channel demodulators, networking (USB, HDMI, Ethernet, SD card reader), 120 Hz, H.264 HD decoding, advanced Picture Quality Algorithms, etc.

- Smallest memory requirement for the total system
  - Full application (networking, H.264 HD decoding, advanced gfx, FRC, …) all on 2x16-bit DDR2 footprint!

- Drives industry's lowest cost-of-ownership/bill-of-material
  - Avoid expensive EMI protection with built-in spread-spectrum on both LVDS as well as DDR interfaces

- Enables development for global chassis roll out thanks to low system costs
  - Minimize upfront development costs and time-to-market for global rollout
  - One development, one PCB line, one test set up
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TV550 System Integration

PNX85500

- CVBS, Y/C, RGB
- L/R
- YCbCr

- TDA10024: DVB-C Channel Decoder
- TDA18272: Tuner
- TDA10048: DVB-T Channel Decoder
- TDA8296: Analog IF IP
- TDA9996: Silicon Tuner Switch
- HDMI Switch

- TFA9810: Audio Amplifier

- NXP PNX8543: MIPS32@300 MHz
- NXP PNX85500: Frame Rate Conversion
- NXP PNX5120: RGB, HV

- DDR2: 256MB, 128MB
- Flash: 128MB

- HDMI, USB, PC - AVI

- SPDIF
- PCMCIA

- HD 1080p 100/120Hz 50/60Hz

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TV550 – FRC 120Hz FULL HD
DVB-T, CI+, PAL/SECAM, IP
TV550 – FRC 120Hz FULL HD
DMB-T/ATSC/ISDB-T, PAL/SECAM/NTSC, IP

Optional China CI+
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Organizational Complexity

- World-wide multi-site project
  - UK, Netherlands, Germany, France, India, Israel, USA

- Number of IPs
  - Approx 100 IP blocks (85% NXP-internal)

- Compute infra metrics
  - 15 TBytes of disk space
  - 3 TBytes of RAM for SoC Integration
Integrating many different functions

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**Function Examples**

- **MIPS24K**
  - Analogue Standards Decoder
  - MPEG Demux & Descrambler
  - Picture Quality Processing
- **Digital Audio Decoder**
  - MPEG/H.264 Video Decoder
  - Frame Rate Conversion
- **Flexible Video Decoder**
  - Auto Picture Control
- **Audio and Video Capture**
  - Video Presentation
- **Audio Post-Processing**
  - Graphics Rendering
- **Connectivity Interfaces**
  - Audio Presentation
- **Audio and Video Capture**
  - Auto Picture Control
Challenging Bandwidth and Latency Needs

Cost pressure only allows 2 x 16 DDR2-1066

- Limiting gross bandwidth to 4.2 Gbytes/sec
- Originally the TV550 system was expected to need 64-bit DDR interface

Requiring high-bandwidth and low-latency

- Processors for flexible processing: requiring low-latency to minimise cache miss penalty
- Hardware traffic mostly predictable: requiring high-bandwidth

Innovative solutions

- Processors supported by specific arbitration settings in infrastructure
- Hardware units and VLIW pre-fetch memory accesses
- Local caches/buffers
- Video streaming between IP functions

Memory Subsystem with Arbitration and Buffering
Assuring fast Silicon Bring-Up
Extensive suite of verification methods

- Various abstraction levels in simulation of
  - IP functionality and connectivity
  - SoC infrastructure performance

- Emulation of representative Software and Hardware
  - 300 million gates of IC emulation capacity
  - System tuning and performance sign-off
  - 300 - 400 k frames of HD video before tape out

- Advance system software development

- All main use-cases had been brought up on the emulator before silicon
  - Software was ready when silicon arrived
  - Arbitration and tuning settings had been verified

=> Very rapid silicon bring-up
PNX85500 Silicon

- TSMC's 45nm Low Power (LP) process technology
- 27 mm Flip Chip BGA Package

- Power Consumption < 7 Watt
- No active cooling required
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Complex SoC made up by Complex IPs
Example: Video Scaler

VCAR
MPEG Artefact Reduction

STDI
De-interlacer

AHSC
Horizontal scaler

TNR
Temporal Noise Reduction

PCOR
Projection data for film detector
Complex SoC made up by Complex IPs
Example: Video Composition Pipe

- PCTI: Peaking-based Color Transient Improvement
- SKCR: Skin-tone Control
- VSHR: Video Sharpening
- BSKY: Blue-Sky Enhancement
- DI2D: 2-Dimensional Backlight Dimming
Motion Accurate Picture Processing
Film Judder Cancellation + Motion Blur Reduction

Original Movie
24 frames per second

Typical TV
at 50 or 60 frames per second
(with ‘movie judder’)

PNX85500 output
at 120 frames per second; after movie judder removal

High quality smooth, natural-looking motion
- analysed and created
- in real-time, for HD video content
- at 120 frames per second
Improved Picture Quality at Reduced Power
2D Local Dimming Processing

- Reduce LCD TV’s backlight power by about 50%
- Significant increase of contrast and black level
- Histogram measurement and pixel processing done in HW-IP
- Flexible processing of VLIW processor for image analysis and backlight calculation
Conclusions

PNX85500: the world’s first DTV SoC in 45nm
• Very high level of integration
• Award-winning 120 Hz processing in front-end TV SoC
• Enabling global chassis, single platform

Performance critical
• Iterative analysis and optimisation through design cycle
• Solving challenging demands on memory latency

Verification challenge
• Very high level of integration creates challenges in interdependency and complexity
• Extensive use of prototyping using emulation and FPGA

First silicon arrived in Q1 2009
• Successful customer demonstrations within 2 weeks of first silicon!

What’s next?
• Higher integration levels, lower system cost
• Improved picture quality, increased frame rates and resolution
• New video features
Questions