HotChips21
Session Six: SoCs + Clocking

SoC for Car Navigation Systems
with a 53.3 GOPS Image Recognition Engine

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Hideaki Kido*, Shoji Muramatsu*,
Yasuhiro Hoshi**, Hiroyuki Hamasaki**,
Atsuhi Nakamura **, Akihiro Yamamoto **

*Hitachi Ltd., **Renesas Technology Corporation
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2. New Image Recognition Engine (IMP-X)
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Advanced car navigation systems will supply multi applications assisting and entertaining our driving.
Demanded Technology for Advanced Car Navigation Systems

**Navigation**

- High Performance and various graphic processing technology
- GPS technology

**Amusement**

- Multimedia interface technology
- Audio / video processing technology

**Safety**

- High performance embedded image recognition technology
- Connection with vehicle-control technology

**fundamental technology**

- High-performance processor
- High speed bus and data I/O technology
- Multi-application support technology
CPU performance

Renesas: No.1 market share worldwide in microcomputer of car navigation systems

For high-end model

SH-Navi3 (SH7776)
CPUx2(533MHz)
2D/3DG., Image Recog., PCI Express, DDR3

SH-Navi2V (SH7774)
CPU(600MHz), 2DG, Vin, Image Recog., DDR2

Image recognition engine (IMP)

Integrating many customer needs and taking future needs in advance

~2005 2006 2007 2008 2009 2010

SH-4A dual core
New image recognition engine (IMP-X)

Products Lineup for 1-Chip Embedded Car Navigation Systems

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Next Generation 1-Chip Solution : SH-Navi3

**SH-Navi3**

- **Core1**
  - SH-4A 533MHz
- **Core2**
  - SH-4A 533MHz

- **2D/3D graphic accelerator**
- **Image recognition processing engine**
- **Video input (3ch)**
- **Display unit (2ch)**
- **DDR3-SDRAM memory interface (2ch)**
- **SuperHyway bus**

For multi-core system
- Support AMP and SMP
- EXREAL Platform™
  1. ExVisor : inter-OS prevention technology (Domain Separation)
  2. ExARIA : inter-OS communication interface (Domain interoperation)

- **In-Car Cameras**
- **External peripheral interfaces**: USB2.0, CAN, PCI Express, ATA, etc...

Diagram:
- **Core1**: SH-4A 533MHz
- **Core2**: SH-4A 533MHz
- **Domain1**
  - App1
  - OS1
  - CPU1
  - ExARIA
  - ExVisor
  - Memory
- **Domain2**
  - App2
  - OS2
  - CPU2

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### Specification of SH-Navi3

<table>
<thead>
<tr>
<th></th>
<th><strong>SH-Navi2V (SH7774)</strong></th>
<th><strong>SH-Navi3 (SH7776)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>90nm</td>
<td>65nm</td>
</tr>
<tr>
<td><strong>CPU</strong></td>
<td>SH-4A&lt;br&gt;600MHz (1080MIPS)&lt;br&gt;FPU : 4.2 GFLOPS</td>
<td>SH-4A x 2&lt;br&gt;533MHz x2 (1920MIPS)&lt;br&gt;FPU : 7.46 GFLOPS</td>
</tr>
<tr>
<td><strong>Cache</strong></td>
<td>I: 32KB, D: 32KB</td>
<td>I: 32KB, D: 32KB, L2: 128KB</td>
</tr>
<tr>
<td><strong>Image recognition engine</strong></td>
<td>38.4 GOPS engine</td>
<td>53.3 GOPS engine&lt;br&gt;Distortion correction module</td>
</tr>
<tr>
<td><strong>Graphics IP</strong></td>
<td>2D accelerator</td>
<td>2D/3D accelerator&lt;br&gt;PowerVR SGX *</td>
</tr>
<tr>
<td><strong>Video in /Display unit</strong></td>
<td>2ch / 1ch</td>
<td>3ch / 2ch</td>
</tr>
<tr>
<td><strong>Temperature range</strong></td>
<td>-40 ~ 85° C</td>
<td>-40 ~ 85° C</td>
</tr>
<tr>
<td><strong>External memory</strong></td>
<td>DDR2 (DDR600)</td>
<td>DDR3 (DDR1066) 2ch</td>
</tr>
<tr>
<td><strong>Transistor count ratio</strong></td>
<td>1.0</td>
<td>2.16</td>
</tr>
</tbody>
</table>

* Imagination Technology Ltd.
Current demands

Object recognition for avoidance of traffic accident
- vehicle, pedestrian, traffic sign, lane, etc...

Making more understandable images
- parking assist etc...

Changing view point with distortion correction

These applications have to be processed in real-time
Real time application with image recognition consumes a lot of computational power

Necessary computational power

Year

Lane Recognition

10,000 [MIPS]

1,000

100

10

Rain Fog Detection etc.

Sign Recognition

Vehicle Detection (Comfort)

Driver Monitoring

Pedestrian Detection (Warning)

Pedestrian Detection (Control)

Vehicle Detection (Control)

Eye Focus Detection

1920MIPS : Max CPU performance of SH-Navi3

Solution : Embedded Image recognition accelerator (IMP-X)
Concepts of Image Recognition Accelerator (IMP-X)

- IMP-X accelerates frequency-used and simple functions
- CPU calculates the others or complicated functions
- IMP-X & CPU access same image memory region with same distance

Process time distribution of image recognition application

Relationship of between IMP-X, CPU, bus, and image memory region
Process Flow of Image Recognition

**C**PU CPU 533MHz x 2

**Video** Input x3

**DDR3** Memory Interface

**Display** Unit x2

**Peripherals**

**SuperHyway bus (266MHz/64bit)**

**SuperHyway bus (133MHz/128bit)**

**IMP-X (266MHz)**

**Local bus**

**Main processing unit**

**Micro code controller**

**local parallel & pipeline processors**

**Post processing unit**

**Histogram processing unit**

**Function specific accelerator (IMR)**

90fps@VGA

**Pre processing unit**

**Line memory**

**Feedback loop**

- Image processing flow
- IMR access
- CPU access

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IMP-X Characteristics

**For High-speed processing**
- Various image functions - up to 53.3 GOPS
- Distortion correct, changing view point

**For Integration into SoC**
- Compact Architecture
- PIPE (Programmable Image Processing Extensions)

**For Versatile processing**
- Local parallel processing
- Pipeline processing
- Function specific accelerator (IMR)
For High-speed Processing : Various Image Functions

What functions does IMP-X accelerate?

- Image Affine Transformation
- Pixel Transformation
- Inter Pixel Arithmetic Calculations
- Inter Pixel Logical Calculations
- Binary Image Shape Transformation
- Convolution

\[ \Rightarrow 0.66 \text{ms@VGA} \]

- Minimum/Maximum Filter
- Rank Filter
- Labeling
- Gray Scale Image Characteristics
- Binary Image Characteristic Extraction

\[ \Rightarrow 1.18 \text{ms@VGA} \]

- Memory Access
- Binary Pipeline Filter
- Pipeline Control
- YUV Color Processing
- Binary Matching Filter
- Optical flow
- Template Matching (SAD, Normalized Correlation etc)
- Matrix operation
- FFT
- etc…

Normalized correlation is operated at **53.3 GOPS** (Max performance of IMP-X)
For High-speed Processing: Template Matching

- Calculate similarity between template pattern \( f(x, y) \) and part of image \( g(x, y) \)

\[
\text{Normalized Correlation} = \frac{\sum \sum (f(x, y) - \bar{f})(g(x, y) - \bar{g})}{\sqrt{\sum \sum (f(x, y) - \bar{f})^2} \times \sqrt{\sum \sum (g(x, y) - \bar{g})^2}}
\]

- Total Processing: \((1+2+2+3)\) Operations * 25 GSEUs * 266 MHz = \text{53.3GOPS}
For High-speed Processing : Distortion Correction

- Generating image pattern for distortion correction, rotation, zoom out/in
  - Control by flexible triangle mesh with vertex data set
- YUV image format (combination/independent), Gray-scale format (8bpp)
- Hi-Speed drawing engine at 90fps with VGA

Raw image from camera

Intensity(Y)plane

Rotation, Zoom-Out

Distortion Correction

Color(UV)plane

Result image

Intensity(Y)plane

Image Recognition

Color Graphic

Function specific accelerator (IMR)
For Integration into SoC and Versatile Processing

- **Programmable processing** at each line with micro-code control
- **Reducing data traffic** between IMP-X and memory by store and reuse of processed data in IMP-X

Comparison of 3 image-functions behavior between non-PIPE and PIPE

* DDR3 transfer performance on SH-Navi3: up to 4.27GB/s
Process Flow of Image Recognition

IMP-X (266MHz)

CPU 533MHz x 2
Video Input x3
DDR3 Memory Interface
Display Unit x2
Peripherals

SuperHyway bus (266MHz/64bit)

SuperHyway bus (133MHz/128bit)

IMP-X (266MHz) 128bit

Local bus

Main processing unit

Micro code controller

Pre processing unit

Line memory

local parallel & pipeline processors

Post processing unit

Histogram processing unit

Function specific accelerator (IMR) 90fps@VGA

Feedback loop

Image processing flow
IMR access
CPU access

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Evaluation for Bus traffic reduction

Harris corner detector requires 14 functions

\[
H = \begin{bmatrix}
\sum I_x^2 & \sum I_x I_y \\
\sum I_x I_y & \sum I_y^2
\end{bmatrix} = \begin{bmatrix} a & b \\ b & c \end{bmatrix}
\]

where \( I_x = \frac{\partial I}{\partial x} \), \( I_y = \frac{\partial I}{\partial y} \)

\[
det(H) = ac - b^2
\]

\[
Trace(H) = a + c
\]

\[
R = det(H) - k Trace(H)^2
\]

Corner

### Process time [ms] vs Total bus utilization [%]

<table>
<thead>
<tr>
<th>Process time [ms]</th>
<th>Total bus utilization [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.25 ms</td>
<td>0.0%</td>
</tr>
<tr>
<td>11.19 ms</td>
<td>10.0%</td>
</tr>
<tr>
<td>31.04 ms</td>
<td>30.0%</td>
</tr>
<tr>
<td>11.23 ms</td>
<td>40.0%</td>
</tr>
</tbody>
</table>

- **without PIPE processing**
- **PIPE processing**

bus utilization = \( \frac{\text{load & store request for DRAM}}{\text{all IMP - X cycles}} \)
Pedestrian Detection is one of the important applications for safety system.

Three-layered neural network is used for recognizing pedestrian pattern.

- 1600 recognition repeats

With CPU...

- 1600 times of neural network processing time: 204 ms
- Total pedestrian detection application processing time: 233 ms
The neural network consists of two matrix product operation stages (1,3) and several mathematical transformation stages (2, 4).

With IMP-X ...

- 1600 times of neural network processing time: 204 ms $\rightarrow$ 8.9 ms
- Total pedestrian detection application processing time: 233 ms $\rightarrow$ 29.4 ms
Summary

SH-Navi3 embeds

- High performance dual RISC processors (1920 MIPS)
- 2D/3D graphic accelerators
- Image recognition engine
  -- High-speed processing (up to 53.3GOPS):
    parallel processing + pipeline architecture + function specific accelerator
  -- Bus traffic reduction & Line programmability:
    PIPE architecture

Achieves a 1-Chip solution for Next-Generation Car Navigation Systems