28nm Generation Programmable Families
7 Series FPGAs
Extensible Processing Platform Family
AMBA AXI4 IP

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Agenda

- Xilinx 7 Series 28 nm Families
- Enhanced Power Efficiency
- Enhanced Logic Density
- Enhanced IO Bandwidth
- Extensible Processing Platform
- Advanced Interconnect System
Xilinx 28nm High Performance Low Power Process

28nm process node
- First wave of 28nm HK/MG devices from fabless Si vendors
- >2x device capacity over 40nm devices
- ~50% total power reduction over 40nm devices

Xilinx 28nm High-Performance, Low-Power process
- High-K Metal Gate (HK/MG)
- Developed by Xilinx and TSMC - optimized for high performance & low power
- 65% lower static power than 28nm variants offering similar performance

<table>
<thead>
<tr>
<th>Process</th>
<th>Xilinx 40nm High Performance</th>
<th>28nm Low Power</th>
<th>28nm High Performance</th>
<th>28nm High Performance Low Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Scheme</td>
<td>SiON/Poly</td>
<td>SiON/Poly</td>
<td>HK/MG</td>
<td>HK/MG</td>
</tr>
<tr>
<td>VCC</td>
<td>1V</td>
<td>1.05V</td>
<td>.85V</td>
<td>1V</td>
</tr>
<tr>
<td>Static Power</td>
<td>&gt;2.5x</td>
<td>1.5x</td>
<td>2x</td>
<td>1.0x</td>
</tr>
<tr>
<td>FPGA Performance*</td>
<td>1.0x</td>
<td>0.9x</td>
<td>1.02x</td>
<td>1.0x</td>
</tr>
</tbody>
</table>

* Estimation of FPGA performance based on Xilinx internal benchmark suite
Xilinx 28nm Total Power Reduction

- New for 28nm – 50% Total Power Reduction from 40 nm
  - Static Power - 65% reduction
    - Xilinx High Performance Low Power Process
  - Dynamic Power – 25% reduction
    - 40nm => 28nm process shrink
  - IO Power – 30% reduction
    - VCCAUX voltage reduction from 2.5V to 1.8V
    - High Speed Transceiver power saving features
    - Single Ended IO (DDR3) power saving features
    - Support for 1.2V, 1.35V for memory standards

- Activity Based Logic Optimization – 20% reduction
  - Available in ISE v12
  - Average 20% savings (benchmark results)
  - Leverages clock gating built into Logic Slice

- Additional Low Power Device Options
  - -1L low power .9V speed grades - 20% power reduction

1) Total Power reduction estimated from Xilinx internal benchmarks (Range 45%-61%)
2) Static power reduction for max VCC, 100 DegC, worst case process
Xilinx Architecture Evolution

- **Unified Architecture Advantages**
  - Rapid deployment of 28nm devices
  - Xilinx IP reuse across all devices
  - FPGA tools optimized for Series 7 architecture
  - 3 families for optimal power, cost, performance

- **1st Step Toward Unification**
  - Virtex-6 and Spartan-6 share compatible 6LUT, DSP48 and IO blocks

- **Two FPGA Base Families**
  - Virtex® FPGAs: 4 LUT based high performance, high density family
  - Spartan® FPGAs: 4 LUT based low cost family
## Unified FPGA Family Architecture

<table>
<thead>
<tr>
<th>Series 7 Family</th>
<th>Artix</th>
<th>Kintex</th>
<th>Virtex</th>
</tr>
</thead>
<tbody>
<tr>
<td>Market</td>
<td>Lowest Power &amp; Cost</td>
<td>Best Price/Performance</td>
<td>Highest System Performance</td>
</tr>
<tr>
<td>Logic Cells</td>
<td>20K - 355K</td>
<td>30K - 410K</td>
<td>285K - 2,000K</td>
</tr>
<tr>
<td>Memory Kbits</td>
<td>720 - 12,060 Kbits</td>
<td>2,340 - 28,620 Kbits</td>
<td>14,760 - 64,800 Kbits</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>40 - 700</td>
<td>120-1,540</td>
<td>700 - 3,960</td>
</tr>
<tr>
<td>Max Transceivers</td>
<td>3.75 Gbps</td>
<td>6.6 Gbps</td>
<td>10.3 Gbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10.3 Gbps</td>
<td>13.1 Gbps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>28.0 Gbps</td>
<td></td>
</tr>
<tr>
<td>External Memory</td>
<td>800 Mbps</td>
<td>2,133 Mbps</td>
<td>2,133 Mbps</td>
</tr>
<tr>
<td>Performance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max Select IO</td>
<td>450</td>
<td>500</td>
<td>1200</td>
</tr>
<tr>
<td>Select IO Voltages</td>
<td>3.3V and below</td>
<td>3.3V and below</td>
<td>3.3V and below</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8V and below</td>
<td>1.8V and below</td>
</tr>
<tr>
<td>Relative Static Power</td>
<td>.5x</td>
<td>1.0x</td>
<td>1.0x</td>
</tr>
<tr>
<td>Relative Performance</td>
<td>.65x</td>
<td>1.0x</td>
<td>1.0x</td>
</tr>
</tbody>
</table>
More than Moore

**Challenge:**
- Frequency scaling is minimal
- Performance gains focused on parallelism (= capacity)
- Moore’s Law only doubles capacity

**Solution:**
- New packaging & assembly methodology

**Result:**
> 2x capacity gains over 40nm devices

<table>
<thead>
<tr>
<th>Family</th>
<th>Capacity Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Artix-7</td>
<td>20K – 355K LCs</td>
</tr>
<tr>
<td>Kintex-7</td>
<td>30K – 410K LCs</td>
</tr>
<tr>
<td>Virtex-7</td>
<td>285K – 2,000K LCs</td>
</tr>
</tbody>
</table>
More than Logic
Family Comparisons: RAM, DSP, I/O BW

Xilinx Virtex 7 Devices - RAM

Xilinx Virtex 7 Devices - DSP

Xilinx Virtex 7 Devices - IOs
Single Ended IOs

Xilinx Virtex 7 Devices - High Speed Serial IO Bandwidth (bidirectional)
High-Speed Transceiver Evolution

- **Challenge:**
  - Increase device BW
  - No increase in total device power
  - XCVR gains from scaling: negligible

- **Solution:**
  - Careful circuit design throughout XCVR
  - Increased Gbps / XCVR
  - More XCVR / Device
  - Low power mode for short channels
  - Lanes share a PLL vs PLL per lane

- **Result:**
  - 60% Increased max device BW
  - Device XCVR power unchanged

### Table: Transceiver Rate (Gbps)

<table>
<thead>
<tr>
<th>Max Rate (Gbps)</th>
<th>GTP</th>
<th>GTX</th>
<th>GTH</th>
<th>GT28</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-6</td>
<td>3.75</td>
<td>10.3125</td>
<td>13.1</td>
<td>28</td>
</tr>
<tr>
<td>Artix™-7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Graph:
- **New 7-Series Family**
  - Virtex™-7 X
  - Kintex™-7 & Virtex™-7 T
  - 28Gbps * Transceivers
  - Transceiver Rate (Gbps)
    - 11.18 Gbps
    - 10.3125 Gbps
    - 3.125 Gbps
    - 3.75 Gbps
  - Max GTPs per Device: 4
  - Max GXs per Device: 56
  - Max GTs per Device: 72
## Single Chip 300G Programmable Bridge

### Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>ASIC/ASSP</th>
<th>Virtex-7 Single Chip</th>
<th>Theoretical Part w/o Power Optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (ASIC Gates)</td>
<td>10 Million</td>
<td>689,920 Logic (~10.3 Million ASIC Gates Equivalent)</td>
<td>689,920 Logic (~10.3 Million ASIC Gates Equivalent)</td>
</tr>
<tr>
<td>IO Bandwidth</td>
<td>1.2 Tbps</td>
<td>1.2 Tbps</td>
<td>1.6 Tbps</td>
</tr>
<tr>
<td>Power</td>
<td>30W</td>
<td>30.4W</td>
<td>42.2W</td>
</tr>
</tbody>
</table>

### Observations

- **28% Power Savings Compared to Device without Power Optimizations**

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*Total Price includes initial ASIC development*
### Challenge
- Cost sensitive mid range market segment
- No compromise in fabric performance

### Solution
- Same process as Virtex-7
  - Same Performance (as Virtex-7)
- Bare die flip chip packages
  - 50% reduced cost (vs Virtex-6)

### Trade Offs
- Restricted max die size
- Reduced max XVER rate

<table>
<thead>
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<td>16</td>
<td></td>
</tr>
<tr>
<td>Transceivers</td>
<td>6.6Gbps</td>
<td>10.3Gbps</td>
</tr>
<tr>
<td>Performance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory</td>
<td>2133Mbps</td>
<td></td>
</tr>
<tr>
<td>Performance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. SelectIO™</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>Select IO Voltages</td>
<td>3.3V and below</td>
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</tr>
</tbody>
</table>
Real World Customer Impact

2x2 LTE Radio

Virtex-6 LX75T

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Virtex-6 LX75T-FF784</th>
<th>Kintex-7 XC7K70T-FBG676</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Cost</td>
<td>1.0</td>
<td>.5</td>
</tr>
<tr>
<td>Sys Performance</td>
<td>368MHz</td>
<td>368MHz</td>
</tr>
<tr>
<td>Power</td>
<td>8.7W</td>
<td>4.48W</td>
</tr>
</tbody>
</table>

Kintex-7 Performance Upgradable to 491MHz
Availability

- Tools available now
- First devices in early 2011
- Solution kits phasing in in late 2011
Xilinx EPP

- **Hybrid SOC + FPGA creates a new product class**
  - Unprecedented configuration compared to an SOC
  - Unprecedented integration compared to an FPGA

- **28nm based product**

- **Significant advantages over a discrete uP + an FPGA**
  - Cost, power, bandwidth and latency

- **Leverages best of ARM and Xilinx Ecosystem**
  - Rich ecosystem of OS, Middleware and Tools support for ARM
  - Tools and IP support for Xilinx FPGA

- **Today: EPP Overview**

- **Future: Detailed family charts, performance numbers, etc**
EPP: An SOC from Xilinx
(Coming from an FPGA company?)

An SOC with an embedded FPGA
- Application level Dual Core ARM A9
- Hard Peripherals
- Cache and Memory
- ASIC-like Cost
- ASIC-like Power
- + 7 Series Programmable Logic

Boots like a Processor
Acts like a Processor
Really ... is a Processor
... and more

Can you find the FPGA?
EPP: Extensible
(the FPGA value add)

- **Extensible I/O Interfaces**
  - Augment the built-in peripheral set
  - Pre-designed standard peripherals
  - User designed custom peripherals

- **High BW Real Time Processing**
  - Video pipelines
  - Low latency, real time events

- **CPU Offload (accelerators)**
  - Xilinx XtremeDSP functions
  - Custom processing functions
  - Up to 0.2 T MAC/s, Up to 2.8 T (int16)

- **CPU Power Offload**
  - ~10x power reduction per operation

- **Hybrid Many Core**
  - Sea of custom processors in PL*
  - OpenCL like machine

*PL = Programmable Logic

**Change the program**
**Customize I/O interfaces**
**Add compute accelerators**
EPP: Processor System

- **Processor System boots first**
  - Separate power for PL*
  - Peripherals alive before PL configuration

- **Processor controls PL configuration**
  - Multiple security levels supported
  - Boot in secure or non-secure mode
  - Download PL image via network, SD, USB

- **Multiple AXI interfaces to PL**
  - Processor System can access IP in PL
  - PL IP has access to Processor System peripherals and memory system at full BW

*PL = Programmable Logic
EPP: Programming

- **Out-of-the-box SW programmable**
  - No FPGA design expertise required

- **Standard OS support**
  - Dual core ARM A9 base platform

- **Many Sources of SW and HW IP**
  - Standardized around AMBA-AXI
  - Xilinx, ARM libraries
  - 3rd Parties

- **Industry-Leading Tools**
  - ARM RVDS Suite & Ecosystem
  - Open source GNU tools
  - Xilinx ISE® Design Suite
  - Xilinx Targeted Design Platforms
Lessons Learned

Past Experience (8 Years)
- MicroBlaze and PowerPC
- Processor IP and HW Tools
- FPGA design centric

Customer Requests
- Out-of-box programmable
- CPU architecture roadmap
- Open standards
- Ecosystem
- Scalable performance

Xilinx EPP Solution
- Processor-centric approach
- Software-centric approach
- ARM® processing engine
- AXI interface standard
- MicroBlaze continues as soft core solution

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PowerPC® is a Registered Trademark of IBM
MicroBlaze® is a Registered Trademark of Xilinx
AMBA AXI
(New interconnect standard for all Xilinx IP)

- Open standard from ARM
  - Well supported, documented and widely adopted
  - Broad set of IP available with AXI interface
  - Royalty free on any target technology

- High performance interface
  - Optimized for frequency, throughput, latency and/or area
  - Supports pipelining with optional register slice
  - QoS controls

- Easy to use
  - One family of interfaces to learn
  - Supports embedded, DSP, and logic users

- Ecosystem
  - Partners are embracing Xilinx’ move to AXI
  - Verification IP available
  - Widely adopted in the ASIC world

- New AXI4 interface variants optimal for FPGA
  - Xilinx contributed to specification process
AXI4 interface variants optimized for area and performance

- **AXI4**: Maximizes data throughput for an interface
- **AXI4-Lite**: Area efficient implementation, used for control and status
- **AXI4-Stream**: Easily connect to non-address based peripherals
AXI4 Transaction Examples

- **AXI4 Base Protocol**
  - Independent read and write interfaces
  - Split transaction
    - Address xfer decoupled from data xfer
  - Simple READY/VALID handshake
  - Data width from 8 to 1024 bits
  - Burst size from 1-256 data beats
  - Pipelined operation
    - ID tags on each channel
    - Overlapping transactions (reads/writes)
    - Out-of-order completion (reads)
    - Interleaving of data beats (reads)

- **AXI4-Lite**
  - Single Transaction only (no burst)

- **AXI4-Stream**
  - Write Data Channel only

**READY/VALID Handshake**

Channel payload

ACLK

VALID

READY
AXI Interconnect IP
(designed by Xilinx, optimized for FPGA)

- **Crossbar**
  - Up to 16 masters and 16 slaves per interconnect
  - Cascadeable (multi layer switches)
  - Independent write and read address arbitration
  - Sparse crossbar data path between configured endpoints

- **Data width, protocol and clock conversion**
  - 32 to 1024 bit data width (256 bit max at launch)
  - Built-in AXI4-Lite and AXI3 protocol conversion
  - Asynchronous and integer-ratio clock conversion

- **Built-in buffering**
  - Pipeline registers per channel to boost frequency
  - Data FIFOs per endpoint for “bursty” throughput

- **Multiple threads (transaction IDs)**
  - Read data reordering and interleaving between threads
  - Reduces stalling

**Optional AXI Register Slice/Buffer**
- Configurable FIFO depth

**Optional AXI Protocol Conversion**
- Data Width conversion
- Protocol Bridge
- Integer-Ratio Clock Bridge
- Asynchronous Clock Bridge
Summary

- **Unified device architecture for all 7 Series FPGAs**
  - Scalable platform with three families: cost, power, performance
  - 50% total power reduction
  - Increased capacity and bandwidth

- **Xilinx EPP: SOC with embedded programmable logic array**
  - Boots like a processor
  - SW centric programming model
  - Extensible peripheral set and compute

- **All Xilinx IP (soft and hard) use AMBA AXI interconnect**
  - High performance, scalable interconnect
  - AXI4 is optimized for FPGAs
  - Memory mapped and streaming interfaces

- **Availability**
  - IP with AXI interface: Sept 2010
  - 7 Series FPGAs: First devices in early 2011
  - EPP: To Be Announced
References

- **Xilinx 28 nm HPL technology**

- **Xilinx Series 7 FPGA Families**
  - [Series 7 Press Backgrounder](http://www.xilinx.com/technology/roadmap/7-series-fpgas.htm)

- **Xilinx Extensible Processing Platform**

- **AMBA-AXI**