Introducing 28-nm Stratix V FPGAs: Built for Bandwidth

Dan Mansur
Sergey Shumarayev
August 2010
Market Dynamics for High-End Systems

Communications
- Mobile Internet driving bandwidth at 50% annualized growth rate
- Fixed footprints
- Existing power ceilings
- 40G/100G system deployment with 400G on the horizon

Broadcast
- Worldwide proliferation of HD/1080p
- Move to digital cinema and 4K2K
- Fixed power budget

Military
- Heightened intelligence and defense needs
- More sensors, higher precision driven to decision points faster
- Power and uptime critical

Computer and Storage
- Higher bandwidth, performance and lower latency
- Power consumption affects total cost of ownership
- Cloud computing driving up bandwidth
Stratix V FPGA Family on 28-nm Process

- Stratix V FPGAs are built on TSMC’s high-performance 28-nm HKMG process
  - Optimized for low power
  - ABB with core voltage 0.85V

- Ideal choice for devices used in next-generation, high-bandwidth systems
  - 35% higher performance than alternative process options
  - 30% lower total power versus previous generations
  - Enables fastest and most power-efficient transceivers
Stratix V FPGAs – Built for Bandwidth

- **Bandwidth**
  - 66 transceivers capable of 12.5 Gbps and 6 x72 800-MHz DDR3 interfaces
  - Devices with 28-Gbps transceivers

- **Integration**
  - Embedded HardCopy Blocks supporting PCI Express Gen3 and 40G/100G Ethernet
  - High-performance, high-precision DSP
  - Enhanced logic fabric with 1,100K LEs, 50 Mb RAM, and 3,510 18x18 multipliers

- **Flexibility**
  - Fine-grain and easy-to-use partial reconfiguration
  - Configuration via PCI Express

- 50% higher system performance and 30% lower total power
# Stratix V Family Plan

<table>
<thead>
<tr>
<th>Device</th>
<th>Interconnect</th>
<th>Hard IP</th>
<th>Core Fabric</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Transceivers (12.5G, 28G)</td>
<td>GPIO</td>
<td>72-bit DDR3</td>
</tr>
<tr>
<td>Stratix V GT FPGA</td>
<td>5SGTB5</td>
<td>32, 4</td>
<td>597</td>
</tr>
<tr>
<td></td>
<td>5SGTB7</td>
<td>32, 4</td>
<td>597</td>
</tr>
<tr>
<td>Stratix V GX FPGA</td>
<td>5SGXA3</td>
<td>36, 0</td>
<td>624</td>
</tr>
<tr>
<td></td>
<td>5SGXA4</td>
<td>36, 0</td>
<td>624</td>
</tr>
<tr>
<td></td>
<td>5SGXA5</td>
<td>48, 0</td>
<td>840</td>
</tr>
<tr>
<td></td>
<td>5SGXA7</td>
<td>48, 0</td>
<td>840</td>
</tr>
<tr>
<td></td>
<td>5SGXB5</td>
<td>66, 0</td>
<td>648</td>
</tr>
<tr>
<td></td>
<td>5SGXB6</td>
<td>66, 0</td>
<td>648</td>
</tr>
<tr>
<td>Stratix V GS FPGA</td>
<td>5SGSB7</td>
<td>27, 0</td>
<td>1032</td>
</tr>
<tr>
<td></td>
<td>5SGSB8</td>
<td>27, 0</td>
<td>1032</td>
</tr>
<tr>
<td>Stratix V E FPGA</td>
<td>5SEB9</td>
<td>-</td>
<td>900</td>
</tr>
<tr>
<td></td>
<td>5SEBA</td>
<td>-</td>
<td>900</td>
</tr>
</tbody>
</table>
Increased Efficiency and System Performance

- **New ALM architecture**
  - Higher logic efficiency and performance
  - 800K additional registers on largest device
  - Ideal for heavily pipelined and register-rich designs

- **New M20K block and MLAB**
  - Improved area efficiency and higher system performance
  - Up to 53 Mbits embedded RAM

- **New fPLLs - high resolution clock synthesis**
  - Replaces board-level clock frequency sources (VCXOs) and reduces clock pins

- **Enhanced routing**
  - Easier timing closure and higher utilization
## Power Techniques

<table>
<thead>
<tr>
<th>Power Reduction Methods</th>
<th>Lower static power</th>
<th>Lower dynamic power</th>
</tr>
</thead>
<tbody>
<tr>
<td>28-nm process changes</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Low power transceivers (200mW @ 28 Gbps)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Programmable Power / Adaptive Body Bias</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Lower core voltage (0.85V)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Extensive hardening of IP, Embedded HardCopy Blocks</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Hard power down of functional blocks</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Clock gating</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Customized extra-low leakage devices</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Partial Reconfiguration</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>DDR3 and dynamic on-chip termination</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
New Embedded HardCopy Block
Flexible Transceiver Architecture

- Scalability and flexibility through a continuous bank of transceivers
- Complete PMA+PCS per channel
- Flexible clocking options with abundant transmit clock sources enabling up to 44 independent data rates

<table>
<thead>
<tr>
<th>Transmit Clock Source</th>
<th>Number</th>
<th>Data Range (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>28G LC PLL</td>
<td>4</td>
<td>20 - 28</td>
</tr>
<tr>
<td>12G LC PLL</td>
<td>22</td>
<td>3.25 - 12.5</td>
</tr>
<tr>
<td>CMU PLL</td>
<td>22</td>
<td>0.6 – 12.5</td>
</tr>
<tr>
<td>Core PLL (fPLL)</td>
<td>22</td>
<td>0.6 – 3.75</td>
</tr>
</tbody>
</table>
## Stratix V Integrated Hard IP

### Embedded HardCopy Block Hard IP

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>x8 PCIe Gen3</td>
<td>PCS, PHY/MAC, data link, transaction layer</td>
</tr>
<tr>
<td>40GE/100GE</td>
<td>MLD/PCS – gearbox, block sync, alignment marker, reorder virtual channel, async buffer/deskew, block striper/destriper, scrambler/descrambler</td>
</tr>
</tbody>
</table>

### Transceiver PCS Hard IP

<table>
<thead>
<tr>
<th>Interface</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interlaken</td>
<td>Gearbox, block sync, 64b/67b, frame sync, scrambler/descrambler, CRC-32, async buffer/deskew</td>
</tr>
<tr>
<td>10GE (10GBASE-R)</td>
<td>Gearbox, block sync, scrambler/descrambler, 64b/66b, rate matcher</td>
</tr>
<tr>
<td>SRIO 2.0</td>
<td>Word aligner, lane sync state machine, deskew, rate matcher</td>
</tr>
<tr>
<td>CPRI/OBSAI</td>
<td>Word aligner, bit slip (deterministic latency)</td>
</tr>
</tbody>
</table>
External Memory Interface

- New UniPHY enables half the latency of ALTMEMPHY
- High system reliability
  - Duty cycle correction
  - Calibration algorithms
  - VT compensated deskew delays
  - PVT tracking mechanisms
- Sharing of PLLs and DLLs across multiple interfaces
- Hard I/O FIFOs and read/write paths
- Ease of use
  - UniPHY available as cleartext
  - Nios processor-based calibration sequencer for easier debug and customization
  - Easy-to-use application of timing and pin constraints
  - Improved documentation
Stratix V Transceivers

August 2010
High-Bandwidth Transceivers

- **28-Gbps transceivers**
  - 20 Gbps to 28 Gbps
  - Up to 4 full-duplex transceiver channels
  - CEI-28G compliant

- **12.5-Gbps transceivers**
  - 150 Mbps to 12.5 Gbps
  - Up to 66 full-duplex transceiver channels
  - SFP+ and 10GBASE-KR compliant

- **Independent transceivers**
  - Change transceiver settings (PMA or PCS) without interrupting other transceiver channels

- **Overcome channel losses**
  - Ultra-low transmit jitter (LC PLL) and excellent jitter tolerance (analog CDR)
  - Four signal-conditioning techniques to compensate for losses
Backplanes and Optical Modules

- Drive 40” backplanes at 12.5 Gbps
  - 10GBASE-KR compliant (IEEE 802.3AP Clause 72)
- Interface to optical modules directly
  - Built in electronic dispersion compensation (EDC)
  - XFP, SFP+, QSFP, and CFP compliance
- Signal conditioning
  - Pre-emphasis and de-emphasis
  - Four-stage continuous time linear equalizer (CTLE)
  - 5-tap decision feedback equalizer (DFE)
  - Adaptive dispersion compensation engine (ADCE)
- On-die instrumentation
  - Monitor eye margin within the receiver
  - Evaluate effectiveness of signal-conditioning techniques
Stratix V FPGA EyeQ Eye Viewer

- Complete vertical and horizontal reconstruction of eye opening
- Uninterrupted data path for live debug capability
- Serial and parallel data verification for live in-system eye reconstruction
- Known pattern not necessary
- Evaluate effectiveness of signal-conditioning techniques
  - Select optimal pre-emphasis, CTLE, and DFE settings for largest eye opening
EyeQ Circuit

- 64 vertical threshold levels
- 32 horizontal phase-interpolator steps
  - 3ps / steps (@ 10Gbps)
- User selectable threshold / PI setting
- Serial bit checker allows for uninterrupted eye reconstruction on live traffic

EQ: Equalizer
PD: Phase Detector
CP: Charge Pump
VCO: Voltage Controlled Oscillator
PI: Phase Interpolator

© 2010 Altera Corporation — Hot Chips 22 2010

ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS & STRATIX are Reg. U.S. Pat. & Tm. Off. and Altera marks in and outside the U.S.
High Bandwidth at Low Power

- Lower power - 50% power reduction at 11.3 Gbps
- A fraction of the power (< 10%) compared to external transceivers
  - 28 Gbps ~200 mW per channel
  - 12.5 Gbps ~170 mW per channel
  - 6.5 Gbps ~ 80 mW per channel
Transceiver Power at 28 Gbps/28 nm

<table>
<thead>
<tr>
<th>28Gbps PMA Power (mW)</th>
<th>Post-LY</th>
<th>Post-LY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Base features</td>
<td>+Optional features</td>
</tr>
<tr>
<td>RX-CTLE</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>RX-DFE (est)</td>
<td></td>
<td>35</td>
</tr>
<tr>
<td>CDR</td>
<td>98</td>
<td>98</td>
</tr>
<tr>
<td>Deserializer</td>
<td>27.8</td>
<td>27.8</td>
</tr>
<tr>
<td>TX driver</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>TX-FFE (6 dB)</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td>Serializer</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>201</td>
<td>247</td>
</tr>
<tr>
<td><strong>FOM (mW/Gbps)</strong></td>
<td>7.18</td>
<td>8.82</td>
</tr>
</tbody>
</table>

- Low-power design enables the 28nm transceiver achieves <= 8.82 mw/Gbps (pJ/bit) power FOM at 28 Gbps
World’s First 28nm Transceiver at 28 Gbps

- Tx eye diagram measured from a 28nm chip
28Gbps Transceiver Physical View
RF Die-Package Design

Inductor are placed strategically under each 28G bump to tune out parasitic loading.
**Signal Conditioning Working**

- Support up to 12.5Gbps data rate
  - For c2c, c2m and backplane

- RX Path (CTLE):
  - 4 EQ stages: up to 20dB programmable AC gain
  - Peaking is independently controlled to meet 6G and 12G BPs
  - Programmable DC gain of 3dB/6dB/9dB/12dB with 3dB/stage

![Graph showing gain vs frequency](image-url)

<table>
<thead>
<tr>
<th>Freq</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.25GHz (6.5Gbps)</td>
<td>Default mode</td>
</tr>
<tr>
<td>6.25GHz (12.5Gbps)</td>
<td>Half bandwidth mode</td>
</tr>
</tbody>
</table>

![Comparison of waveforms with and without equalizer](image-url)

- Measured Results (actual)
28-nm Transceiver Demonstration Board

(1) 2.4mm MMPX Connectors (20+ Gbps Channel)
(2) 28-nm Transceiver Demonstration Device
(3) 3.5mm SMA Connectors (12.5 Gbps Channel)
(4) FCI Airmax VS® Backplane Connectors
(5) Programmable Clock Oscillator