Taking semiconductors to the next level

3D FPGA & 3D ASIC

Worlds first unified 3D IC design platform

Raminda Madurawe
Hot Chips, August 2010
2D FPGA dilemma

• Large programming overhead
  ▪ Longer wires = degradation
  ▪ Removing overhead = 2\textsuperscript{nd} design

• 20 years of SRAM scaling
  ▪ CRAM > memory SRAM
  ▪ Stability / disturb at 28nm?

CRAM = configuration SRAM

C/RAM & SRAM scaling

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3D Product concepts

- **2D FPGA** – poor area, cost, power, speed
- **3D FPGA** – better area, power, cost, speed
  - Same placement / wires / base die
  - One design – **one timing closure** – FPGA/ASIC options
"Bitstream" timing closure

TierFPGA
- TFT SRAM

TierASIC
- Metal ROM

MultiASIC™
- TFT MUX

Dynamic Signals

Static Control

One bitstream = identical timing = deterministic

Base die
Monolithic process

- TFT SRAM/MUX over CMOS
  - FPGA fabric / FPGA tools
  - Temperature < 400 °C

- Metal ROM over CMOS
  - FPGA fabric / FPGA tools
  - “Bitstream” custom M9

(Images of circuits showing TFT and metal layers)
Thin-film-transistors (TFT)

- **N/P thin-film transistors**
  - Majority carrier
  - Accumulation mode

- **9-TFT SRAM cell**
  - \(< 10\mu W\) static / \(10^6\) bits
  - \(I_{ON} / I_{OFF}\) stable & durable
TFT SRAM latches

• Static circuits
• $V_T$ not critical
• Low power
E-field scalable

- 90nm CMOS – TFTs operate at 3.3V
- 45nm CMOS – TFTs operate at 1.8V
- Scale with CMOS
Improving gate density

- Approach ASIC gate density
- Improved mobility switch fabric – laser crystallization

2D FPGA

3D FPGA
  - FPGA
  - Low ROI IC’s

Tru3D
  - FPGA
  - ASSP / ASIC

2D FPGA

Competition

2010

2012 ?

Hot Chips 2010

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Competitive evolution

- Multi-faceted technology evolution
  - 3.5x 3D FPGA
  - 7x Tru3D
- Programmability – as needed – iterative
- Fixed function – when satisfied
- All future ICs will need programmability
- 56 issued patents
4LUT gate density

2D FPGA 4LUT density: follow Moore’s Law
- 180nm = 110/mm² (FY2000)
- 20nm ~ 4500/mm² (FY2013)
- 6 nodes ~ 40x

3D gives higher 4LUTs
- 28 nm = 16k /mm² (FY2013)
# Routing architecture

## Area:
- CR = CRAM
- LO = Logic
- RO = Routing

<table>
<thead>
<tr>
<th>ARCHITECTURE</th>
<th>2D FPGA</th>
<th>ASIC</th>
<th>2D FPGA (No CR)</th>
<th>3D FPGA (3D CR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic cell area</td>
<td>1</td>
<td>e = 0.208</td>
<td>f = 0.313</td>
<td>g = 1</td>
</tr>
<tr>
<td>Wires / area</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>RO per wire</td>
<td>0.6 / N</td>
<td>0.4 / N</td>
<td>0.6 / N</td>
<td>0.665 / N</td>
</tr>
<tr>
<td>LO area</td>
<td>0.125</td>
<td>0.125</td>
<td>0.125</td>
<td>0.335</td>
</tr>
<tr>
<td>RO area</td>
<td>RO₁ = 0.6</td>
<td>RO₂ = 0.4*e</td>
<td>RO₃ = 0.6*f</td>
<td>RO₄ = 0.665</td>
</tr>
<tr>
<td>Area (RO+LO+CR)</td>
<td>1 = CR+LO+RO₁</td>
<td>e = LO+RO₂</td>
<td>f = LO+RO₃</td>
<td>g = LO+RO₄</td>
</tr>
</tbody>
</table>

- LO ratio to 2D: 1.0
- LO Efficiency: 4.8
- User LO / area: 28.8
Unified tools

- FPGA RTL design entry
  - Mentor “Precision” synthesis
  - Tier Logic “Mobius” P&R
- One tool – one placement
  - “Bitstream” for FPGA
  - “M9 mask” for ASIC
- Excellent quality of results
- Combining tools, design & process
FPGA design for ASICS

- FPGA verified RTL
- Standard front end tools
  - No re-design
  - TierFPGA to re-verify (if necessary)
  - Pin compatible TierASICs (6 weeks + $50k)
**Die stack vs. monolithic**

Reference: 3rd Stanford and Tohoku Universities joint Open Workshop on 3D Transistors and its Applications December 2009

- FPGA’s need > 90% area for wires
- 40nm 2D CRAM bit density ~ 90M/cm²
  - Requirement for Via > 1B/cm²

Monolithic Stacking
Vertical interconnect pitch > 200 nm
Vertical interconnect density ~ 2B/cm²
Connect at device level

Limits the vertical interconnect density to $10^5 - 10^6$ /mm²

K. W. Guarini et al., IEDM 2002
S Gupta et al., VMIC 2005
A. W. Topol et al., IEDM 2005

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Summary

• Unified IC design for FPGA & ASIC
  – Beyond process scaling
  – “Bitstream” concept to IC design

• Worlds first monolithic 3D FPGA
  – Same “netlist / placement / base-die” → 3D ASIC
  – Fine grain for logic & course grain for routing

• Augment programmability to ASIC density
  – High mobility 3D nTFT switches

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