Power Management of the Third Generation Intel Core Micro Architecture formerly codenamed Ivy Bridge

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Varghese George, Inder Sodhi, Ryan Wells
Contents

- Ivy Bridge Overview
- Power Scaling & Efficiency
- Idle power Management
- Configurable TDP
- Clocking
- Additional Information
Intel’s Tick-Tock Philosophy

- **Tock Processors**
  - Provide substantial microarchitecture improvement…
  - …on existing manufacturing process

- **Tick Processors**
  - Retain existing microarchitecture, …
  - …but utilize next generation fabrication technology to drive high volume and low product cost

- **The Tock: Sandy Bridge**
  - Brought new ring/LLC microarchitecture
  - Integrated Graphics on ring
  - Integrated North Bridge (“System Agent”), including memory controller

- **The Tick: Ivy Bridge**
  - Process lead vehicle: Intel’s 22nm process node
  - The Caveat:
    - Some Ivy Bridge areas have substantial (tock-like) change (Graphics)
Ivy Bridge – the 1st 22 nm Core Product

- **Leveraged from Sandy Bridge:**
  - Continue the 2-chip platform partition (CPU + PCH)
  - Fully integrated on silicon:
    - 2-4 IA Cores
    - Processor Graphics, Media, Display Engine
    - Integrated Memory Controller
    - PCIe Controllers
    - Modular On-Die Ring Interconnect
    - Shared LLC between IA Cores and Graphics
  - Same socket, similar packages
    - Similar SKUs (TDP, die configurations)
  - IVB backwards compatible with SNB
Ivy Bridge – Key New Things

- Entire chip moves to 22nm
  - Higher performance/Lower power

- Instruction Set Architecture Enhancements
  - Float16 / Fast FS/GS support / REP MOVSB / RDRAND

- Security Enhancements
  - DRNG / SMEP

- Power Improvements
  - Scalability features: ConfigTDP
  - Average Power features: DDR power gates / PAIR

- IO/Memory
  - DDR3L support
  - Improved overclocking support

- Performance Improvements (Instructions/clock)
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Power efficiency via scaling & testing

- Power Scaling in 22nm process extracted in two ways
  - Higher performance in IA & Graphics within a power envelope
  - Lower operating Voltage in System Agent and Memory controller

- Power loss from discrete test points and interpolation (blue line)
- Ivy Bridge builds a quadratic model of the VF based on enhanced testing (red line)
- Optimal voltage at all operating points
Power efficiency via interrupt routing

- **PAIR algorithm lowers power or performance impact of re-routable interrupts**
  - Compares power-state of all cores eligible to service interrupt
  - Chooses “best core” based on optimization mode (Power vs. Performance)
  - “Best Core” based on the following
    - Core C-states
    - P-state request (turbo vs. non-turbo)

- **Example: 1 core in C6 & 1 in C0**
  - Power bias will direct the interrupt to core in C0
  - Performance bias will wake the C6 core
Temperature effects

- Thermal sensors are located in the hot spots in the IA core and GPU core
- Inverse temperature dependence (ITD) effects more pronounced in the 22nm node
  - No sensors at the cold spots
  - IVB estimates the coldest point on the die to based on thermal sensors compensate for the effect
- Manufacturing test voltages at hot and cold temperatures
  - PCU interpolates linearly at run time to determine the voltage
  - Temperature moves slowly enough for the PCU and voltage regulator to keep up
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Ivy Bridge Power Planes

- **Key Power planes**
  - Core (Gated – Green)
  - LLC (Ungated – Purple)
  - SA/Display - Red
  - GT - Blue
  - Others (like IO, PLL etc) - Gray
Ivy Bridge has 3 on-die power gating areas

- Cores (Green)
  - Independent Gating per Core
  - Unified Cache
- PCIE controller (Red)
  - Gating static only when no connection
- DDR (Purple)
  - Gating of digital logic in the buffer applied during self-refresh mode
IREM images

1 core in turbo, other 3 cores power gated

Typical Usage of Cores and Graphics

Cores and Graphics gated
DDR I/O Power Gating

- Ivy Bridge implements on-die Embedded Power Gating (EPG) on DDR I/O

Latency & Tradeoffs

- Latency considerations
  - Enabled on entry into Package C3 and deeper (memory in Self Refresh) to deal with latency of power gate
  - Additional latency of <5μS for device access to memory during exit
  - Conditional enabling – only if devices can tolerate the latency
  - No Impact to exit latency for interrupts

- Design tradeoffs
  - To get around saving and restoring context, the DDR state is put on an ungated power island

- For Idle/MM07-OP, Intel expects DDR IO to be gated ~90% of the time
Low Voltage optimizations

- Small Signal arrays and register files limit the lowest operating voltage and retention voltage

1. Dynamic cache sizing to achieve a lower cache $V_{min}$
   - Cache $V_{min}$ is limited by ‘bad cells’ or defects distributed across the cache
   - A smaller size cache has a lower $V_{min}$ due to fewer defects

2. PCU Firmware based register file re-initialization on exit from standby states
   - Allows reduction of retention voltage below the retention level of the register file
LLC - Dynamic Cache Shrink Feature

- Reduce LLC cache size dynamically from 8MB to 512KB to gain 30mV Vmin benefit
- LLC Expand/Shrink algorithm is developed for this purpose
- Entry/exit points were defined based on the work loads & performance
### LLC - Dynamic Cache Shrink Feature

- **LLC organized in 16 ways.**
- **When PCU detects low activity workload**
  - Flushes 14 ways of the cache and puts ways to sleep
  - Shrinks active ways from 16 to 2 to improve VccMin
- **When PCU detects high activity**
  - Expands active ways back to 16 to improve cache hit rate.

#### Way 1 - Way 16

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<td>Active</td>
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[Image of LLC organization and activity states]
Ivy Bridge average power reduction (relative to SNB)

Power reduction via new PM features and process scaling benefits

Benefits on other SKUs varies
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Configurable TDP & Low Power Mode

- Configurable TDP allows multiple TDP levels within the same part
  - Greater dynamic range of power/performance guaranteed by Intel
  - Dynamically transition based on runtime triggers
- Low Power Mode defines lowest active operating point for the part
- Intel offers software driver implementing both features
  - System designers can utilize this framework and customize to their needs
- Allow OEMs and End Users to take advantage of scalability of Intel CPUs

Higher Performance

'TDP Up'

Nominal

'TDP Down'

Cool and Quiet
Regulated power limit adjusted in conjunction with TDP to allow guaranteed frequency (performance) at a specific power level.
IA/GPU Power sharing

- OEMs can configure the cooling limits to <17W
  - Static biasing (X% to GPU and 100-X% to IA) results in sub optimal performance
- Solution: Distribute power based on workload demand
  - Determine target CPU/ring frequency based on workload
    - If actual CPU/ring freq < (target frequency – guard band)
      - Move bias toward CPU Else Move bias toward GPU
    - With hysteresis
Intelligent Bias Control Architecture
Platform Power management

- **Power delivery management**
  - How do we deal with the platform need to divert current from the CPU to other components dynamically?
    - IVB PCU will manage the current draw and will honor dynamic max current updates

- **Platform debug and tuning hooks**
  - IVB provides feedback to platform designers if power delivery, & cooling is limiting performance
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IVB Clock Domains

Display Reference
120 MHz (100MHz DFx)

Display Port (DP) PLL

IO – 2.7 GHz / 2.5 GHz (DFX)
Logic – 162 / 270 MHz

FDI PLL

IO – 1.62 / 2.7GHz
Logic – 162 / 270 MHz

PCU PLL

MC / DDR PLL

PCIe PLLs

IO – 2.5/5 GHz
LCLK – 250/500 MHz

GDXC PLL

IO 2.5 GHz/5GHz
LCLK 250 Mhz/500 Mhz

RCLKPLL

RCLK
200 Mhz (or)
100 Mhz

Core0 PLL

GT PLL

DCLK – 400/533/667/800 MHz
QCLK – 0.8/1.067/1.34/1.6 GHz

PCU – 1600MHz
SA – 800MHz
DE – 400/800 Mhz

UCLK = Scalable Freq in 100MHz steps
Scalable Freq in 50MHz steps
PLL/Clocking

Clock Islands in Core
Each Island can be independently clock gated.

Clock Islands in Core = 180
Clock Islands in LLC = 48

<table>
<thead>
<tr>
<th>Slice Clocking Cdyn</th>
<th>CORE (pF)</th>
<th>L3 (pF)</th>
<th>TOTAL (pF)</th>
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<tr>
<td>Total (including RT)</td>
<td>179</td>
<td>77</td>
<td>256</td>
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<td>Global Drivers + Islands</td>
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<td>Clock Source + Spines</td>
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<tr>
<td>Silicon Measurement</td>
<td>181</td>
<td>81</td>
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- Wide Range SB PLL
- PCIE LC PLL
- Single Ratio SB PLL
Overclocking Enhancements

- **Core Frequency**
  - Unlocked turbo limits
  - Unlocked core ratios up to 63 in 100MHz increments†
  - Programmable voltage offset

- **Graphics Frequency**
  - Unlocked graphics turbo limits
  - Unlocked graphics ratios up to 60 in 50MHz increments
  - Programmable voltage offset

- **Memory Ratio**
  - Unlocked memory controller
  - Granularity options for 200 and 266MHz
  - Logical support up to 2666MHz

- **DMICLK (aka BCLK)**
  - Unlocked PCH clock controller (1MHz increments)

- **PEG and DMI**
  - Fixed ratios
Real-Time Overclocking

- PCU samples OC parameters continuously and updates power limits.
- OC without reboot:
  - Maximum Core Ratio
  - Processor Graphics Ratio
  - BCLK (small increments)
  - Power Limits: PL1, PL2, Tau
  - Additional Turbo Voltage for CPU and pGfx

Changes effective immediately

Within the OS
Acknowledgements

- Authors would like to thank the entire Ivy Bridge team for their dedicated work.
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Ivy Bridge ISA & Security enhancements
Float16 Data Conversion Instructions

- New instructions for supporting conversion between a 16-bit floating point memory format and 32-bit single precision
  - VCVTPH2PS, VCVTPS2PH
  - Both 128 (SSE) and 256 bit (AVX) wide vector flavors supported
  - Only supported in the VEX prefix context

- Facilitates use of single-precision floating point computations from a more compressed memory format
  - 1-bit sign, 5-bit exponent, 10-bit significand (+ implicit integer bit)

- Enables higher dynamic range compared to fixed point within the same storage footprint
  - Image processing, video decode, audio processing
  - 50% reduction in storage v. single-precision FP (w/ loss of fidelity)

- Enumerated via new CPUID feature flag
  - CPUID.1.ECX[29]
VCVTPH2PS – Convert 16-bit float to SP

VCVTPH2PS \textit{ymm1, xmm2/mem128} - 256 bit vector
VCVTPH2PS \textit{xmm1, xmm2/mem64} - 128 bit vector

Converts four packed 16-bit floating-point values in the low 64 bits of XMM2 or 64-bit memory location to four single-precision floating-point values and writes the results in the destination (XMM1 register).

![Diagram of VCVTPH2PS operation]

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<tr>
<th>127</th>
<th>96</th>
<th>95</th>
<th>64</th>
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<td>VCVTPH2PS \textit{xmm1, xmm2/mem64}</td>
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- xmm2/mem64
- \textit{xmm1}
- \textit{convert}
- VS3
- VS2
- VS1
- VS0
VCVTPS2PH – Convert SP to 16-bit float

VCVTPS2PH \( x_{mm1/mem64}, x_{mm2}, \text{imm8} \) - 128 bit vector
VCVTPS2PH \( x_{mm1/mem128}, y_{mm2}, \text{imm8} \) - 256 bit vector

Converts four packed single-precision floating-point values in XMM2 to four 16-bit floating-point values and writes the results in the destination (XMM1 register or memory location).
Write/Read FS/GS Base Instructions

- New ring-3 instructions for read/write of the FS & GS segment base registers
  - To be used by user level code for thread local storage
  - Enumerated via new CPUID feature flag
    - CPUID.7.0.EBX[0] indicates availability (leaf 7, subleaf 0)
  - Requires enabling by OS to permit FS/GS segment base access
    - CR4.RDWRGSFS (bit 16) = 0 (default)

- Motivation:
  - Improve scalability and programming ease for user threads

REP MOVSB/STOSB improvements

- Historically optimizing block copy/fill operations tends to be microarchitecture specific
  - Lack of a “one size fits all” solution implies CPU model specific algorithms for best performance
- IVB address this through more optimized REP MOVSB and REP STOSB instructions
  - Expect this to replace the need for manual tuning solutions
  - Limitation: If block size is known at compile time and size <=64 bytes, then scalar loads & stores are still considered faster

- Enhancement availability indicated by CPUID.7.0.EBX[9] (ENFSTRG)
  - This bit can be used by run time SW (Libraries, JIT) for tuning to a specific implementation
Background:

- Entropy is valuable in a variety of uses – Example: “keying material” in cryptography
- Historically, computing platforms did not have a good source of a high quality/high performance “entropy source”
- Typical sources used today are slow (bit rate in Kb/s) (key strokes, mouse clicks etc)

IVB introduces high quality/high performance DRNG

The DRNG is designed to be Standards compliant

- ANSI X9.82,NIST SP 800-90 and NIST FIPS 140-2/3 Level 2 certifiable entropy source

New instruction: RDRAND – Available at all privilege levels/operating modes

- Instruction will return a random number (16, 32 or 64-bit) to the destination register

New CPUID feature flag for RDRAND enumeration

CPUID.1.ECX[30]
Supervisory Mode Execute Protection (SMEP)

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**Background:**

- Privilege Escalation Attack causes CPL 0 access to user mode pages
- Example:
  - Step 1: Compromise user mode app or trick user into installing attack app
  - Step 2: Exploit OS vulnerability to force control transfer to user mode attack code while CPU remains in supervisory mode => privilege escalation

**IVB introduces SMEP to help prevent such attacks**

- Prevents execution of user mode pages while in supervisor mode
- If CR4.SMEP set to 1 and in supervisor mode (CPL<3), instructions may not be executed from a linear address for which the user mode flag is 1
- Available in both 32- and 64-bit operating modes
- SMEP is enumerated via CPUID.7.0.EBX[7]
PCI Express Gen 3
Ivy Bridge PCI Express Gen 3

- Third generation of the PCI Express I/O interface
  - Delivers nearly twice the I/O bandwidth v. Gen 2
  - Improves performance for applications sensitive to I/O bandwidth
    - Enables smaller form factors via narrower, faster physical links

- Bandwidth realized through:
  - Faster signaling speed: 8 GT/s
  - More efficient lane encoding: 128/130

- Utilizes Gen 2 I/O channel characteristics
  - Enables compatibility with previous Gen components
  - Enables drop-in upgrade for Sandy Bridge-based platforms

- Supports PCIe bandwidth management & ASPM states
  - Dynamic Link Width Configuration, L0s (Rx & Tx), L1
Ivy Bridge PCIe Performance*

Ivy Bridge delivers nearly 2x Gen 2 bandwidth

- At similar latencies
  - ~300ns typical for upstream read request

Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.
• Sandy Bridge PCIe uArch unchanged
  ▪ No change to primary channel hub/TL interface
  ▪ No change to controller/PHY lanes interface

• Gen 3 changes layered on top of Gen 2 functionality (additional states, arcs)
  • Parallel flows implemented where feasible
IPC Improvements
Most Significant IVB IPC Improvements

- **Pipeline MOV elimination**
  - Eliminates Move related micro-operations from the processor execution pipeline

- **Pipelined divider**
  - Improves throughput of divide related computations

- **Next page prefetcher**
  - Enables prefetching to span across a 4K page boundary

- **Shift/Rotate performance**
  - Addresses glass jaw concern with crypto and hashing algorithms
  - Addresses clumsiness of partial flag handling

- **6 additional split load registers**
  - Improves performance for loads splitting cache lines
  - Especially critical for AVX or SSE
Uncore IPC Features

- **AFP – Adaptive Fill Policy**
  - Cache heuristics to identify and segregate streaming applications

- **QLRU – Quad-Age LRU algorithm**
  - Allows fine-grain “age assignment” on cache allocation
  - E.g.: prefetched requests are allocated at “middle age”

- **DPT – Dynamic Prefetch Throttling**
  - Real-time memory bandwidth monitor
  - Directs core prefetchers to reduce prefetch aggressiveness during high memory load scenarios

- **Channel Hashing -- DRAM channel selection mechanism**
  - Allows channel selection to be made based on multiple address bits
  - Historically, it had been “A[6]”
  - Allows more even distribution of memory accesses across channels
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