Intel® Xeon Phi™ coprocessor
(codename Knights Corner)

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Available on select Intel® Core™ Intel® Xeon® and Intel® Xeon Phi™ processors. Requires an Intel® HT Technology-enabled system. Consult your PC manufacturer. Performance will vary depending on the specific hardware and software used. For more information including details on which processors support HT Technology, visit http://www.intel.com/technology/ht.

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Intel® Many Integrated Core (Intel MIC) Architecture

Targeted at highly parallel HPC workloads
  • Physics, Chemistry, Biology, Financial Services

Power efficient cores, support for parallelism
  • Cores: less speculation, threads, wider SIMD
  • Scalability: high BW on die interconnect and memory

General Purpose Programming Environment
  • Runs Linux (full service, open source OS)
  • Runs applications written in Fortran, C, C++, ...
  • Supports X86 memory model, IEEE 754
  • x86 collateral (libraries, compilers, Intel® VTune™ debuggers, etc)
Knights Corner Coprocessor

Intel® Xeon® Processor
PCIe x16
> 8GB GDDR5 memory
TCP/IP
System Memory

KNC Card

> 50 Cores
Linux OS

>= 8GB GDDR5 memory
GDDR5 Channel
GDDR5 Channel
Knights Corner – Power Efficient

Performance per Watt of a prototype Knights Corner Cluster compared to the 2 Top Graphics Accelerated Clusters

Intel Corp
Knights Corner
Top500 #150
72.9 kW

Nagasaki Univ.
ATI Radeon
Top500 #456
47 kW

Barcelona Supercomputing Center
Nvidia Tesla 2090
Top500 #177
81.5 kW

Higher is Better Source: www.green500.org
Knights Corner Core

X86 specific logic < 2% of core + L2 area
Vector Processing Unit

PPF  PF  D0  D1  D2  E  WB  D2  E  VC1  VC2  V1-V4  WB

D2  E  VC1  VC2  V1  V2  V3  V4

DEC  VPU RF 3R, 1W  LD  EMU  ST  Mask RF  Scatter Gather

Vector ALUs
16 Wide x 32 bit
8 Wide x 64 bit
Fused Multiply Add

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Distributed Tag Directories

Tag Directories track cache-lines in all L2s
Interconnect: 2X AD/AK
Multi-threaded Triad – Saturation for 1 AD/AK Ring

Simulation Data indicates saturation for a single AD/AK ring.

Results measured in development labs at Intel on Knights Corner prototype hardware and systems. For more information go to http://www.intel.com/performance
Multi-threaded Triad – Benefit of Doubling AD/AK

Results measured in development labs at Intel on Knights Corner prototype hardware and systems. For more information go to http://www.intel.com/performance
Streams Triad
for (i=0; i<HUGE; i++)
    A[i] = k*B[i] + C[i];

Without Streaming Stores
Read A, B, C, Write A
256 Bytes transferred to/from memory per iteration

With Streaming Stores
Read B, C, Write A
192 Bytes transferred to/from memory per iteration
Multi-threaded Triad — with Streaming Stores

Results measured in development labs at Intel on Knights Corner prototype hardware and systems. For more information go to [http://www.intel.com/performance](http://www.intel.com/performance)

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Cache Hierarchy Micro-architecture Choices

L2 TLB
   64 entry, holds PTEs and PDEs vs. no L2 TLB

Dcache Capability
   Simultaneous 512b load and 512b store vs. 1 load or store per cycle

L2 Cache
   512 KB vs. 256 KB

Hardware Prefetcher
   16 stream detectors, prefetch into the L2 vs. no HWP (rely only on software prefetching)
Per-Core ST Performance Improvement (per cycle)

Spec FP 2006

Performance impact of KNC core uArch improvements

>1.8x Average Performance/Cycle Improvement – 1 Core, 1 Thread

Results measured in development labs at Intel on Knights Corner and Knights Ferry prototype hardware and systems. For more information go to http://www.intel.com/performance
Caches – For or Against?

Caches:
- high data BW
- low energy per byte of data supplied
- programmer friendly (coherence just works)

Coherent Caches are a key MIC Architecture Advantage

Results have been simulated and are provided for informational purposes only. Results were derived using simulations run on an architecture simulator or model. Any difference in system hardware or software design or configuration may affect actual performance.
Example: Stencils

spatial time-step simulation of a physical system

Cache blocking promotes much higher performance and performance/watt vs. memory streaming
Power Management: All On and Running
When all 4T on a core have halted, core clock gates itself.
Core C6: Power Gate Core

C1 time-out, power gate core, save leakage, requires core-re-init
Timeout when all cores have been in C6, clock gate the L2 and interconnect
Host Driver can initiate Package C6 – Uncore Voltage Off, requires partial restart
Summary

Intel® Xeon Phi™ coprocessor provides:

Performance and Performance/Watt for highly parallel HPC with cores, threads, wide-SIMD, caches, memory BW

Intel Architecture

general purpose programming environment
advanced power management technology

KNC delivers programmability and performance/watt for highly parallel HPC
Thank You

Knights Corner brought to you by:

IAG (Intel Architecture Group)
  • DCSG (Data Center and Systems Group)
  • VPG (Visual and Parallel Group) MIC
    – HW Architecture
    – HW Design
    – SW

SSG (Software and Services Group) MIC

IL PCL (Intel Labs – Parallel Computing Lab)
Vector Processor: 512b SIMD Width

16 wide SP SIMD, 8 wide DP SIMD
2:1 Ratio good for circuit optimization

Shared Multiplier Circuit for SP/DP
Gather/Scatter Address Machinery

Gather Instruction Loop

gather-prime
loop: gather-step; jump-mask-not-zero loop

Scalar Register
Base Address

Vector Register

Mask Register

Clear

Find First

Access Address

To TLB/DCACHE

Gather/Scatter machine takes advantage of cache-line locality
Host Driver Initiated – L2/Ring/TDs dropped to retention V, memory in self refresh