FPGAs with 28Gb/s Transceivers Built with Heterogeneous Stacked-Silicon Interconnects

Ephrem Wu and Suresh Ramalingam
400Gb/s Line Card Application

Up to 16 x 28 Gb/s GTZ Transceivers

Up to 72 x 13.1 Gb/s GTH Transceivers

Line Card

Switch Card

Virtex-7 HT

Network Processor

Fabric Interface

Packet Queues and Lookup Memory (SRAM, TCAM, DRAM)
Heterogeneous Stacked-Silicon FPGAs

Interposer Floorplans

**XC7VH290T**
- **GTZ-IC** (8x28Gb/s)
- **GTH**
- **FPGA**

**XC7VH580T**
- **GTZ-IC** (8x28Gb/s)
- **GTH**
- **FPGA**

**XC7VH870T**
- **GTZ-IC** (8x28Gb/s)
- **GTH**
- **FPGA**

<table>
<thead>
<tr>
<th>Network</th>
<th>2 x 100 Gb/s</th>
<th>2 x 100 Gb/s</th>
<th>4 x 100 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTZ (28G)</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>GTH (13G)</td>
<td>24</td>
<td>48</td>
<td>72</td>
</tr>
</tbody>
</table>

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XC7VH580T Under the Hood

Industry’s First Heterogeneous FPGA
XC7VH580T Under the Hood
Industry’s First Heterogeneous FPGA
XC7VH580T Under the Hood
Industry’s First Heterogeneous FPGA
Two Interconnect Types

Type I
Between IC and Package

Type II
Between two ICs

GTZ-IC

FPGA

FPGA

Passive Silicon Interposer

Microbumps

C4 Bumps

Through-Silicon Via (TSV)

Ceramic Package Substrate

BGA Balls
Packaging, Assembly, and Test

Top Dice, Interposer, & Package

28nm FPGA & Interposer

μBump, Die separation
Joining, & Assembly

Final Test of Packaged Part

Package Substrate
Type I Example: 28 Gb/s Serial Transmitter

Simulated

- Time [ps]
- 25.00
- 37.50
- 50.00
Type I Example: 28 Gb/s Serial Transmitter

Simulated

Actual
Type II Interconnects
Inter-IC Interconnect Microstrip Layout with Side Shields

IC 1
IC 2
Type II Interconnects

Inter-IC Interconnect Microstrip Layout with Side Shields

IC 1

IC 2

Microbump Pad
Type II Interconnects
Inter-IC Interconnect Microstrip Layout with Side Shields

IC 1

IC 2

Microbump
Pad

Microbump
Type II Interconnects
Inter-IC Interconnect Microstrip Layout with Side Shields

IC 1

Microbump
Pad

IC 2

Microbump

Microbump
Pad
Type II Interconnects

Inter-IC Interconnect Microstrip Layout with Side Shields

Interposer

(Dimensions Not to Scale to Show Interconnect Cross Section)
Type II Interconnects
Inter-IC Interconnect Microstrip Layout with Side Shields

Interposer
(Dimensions Not to Scale to Show Interconnect Cross Section)
Wire Length Distribution
Between GTZ-IC and FPGA

Wire Length Histogram

Number of Wires

Cumulative Wirelength Distribution (%)

Wire Length Bin (µm)

4138 Nets Total

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RC Static Timing Analysis for Productivity
Calibrated RC-Based STA Against RLC-Based SPICE

![Diagram]

- GND
- Type II Signal
- GND
- Type II Signal
- GND
- Type II Signal
- GND

RLC → SPICE

RC → Static Timing Analyzer
Summary

1. Presented industry’s first heterogeneous 3D FPGA.

2. FPGA & GTZ-IC create three scalable products.


4. Showed Type I signaling: 28 Gb/s TX over TSVs.

5. Lacked 3D timing tools for Type II signals. Leveraged STA tools calibrated with RLC SPICE runs.