Medfield Smartphone SOC
Intel® Atom™ Z2460
Processor

Rumi Zahir
Intel Corporation
Outline

- Low power platform progression
- Medfield platform for the Smartphone form-factor
  - Constraints, Ingredients, Package
- Penwell SOC
  - Block Diagram
  - Intel Atom™ CPU power management
  - SOC power management
  - Power management software architecture
- Medfield reference platform
- Smartphone roadmap
Low Power Platform Progression

<table>
<thead>
<tr>
<th></th>
<th>Moorestown (45nm)</th>
<th>Medfield (32nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Board size</strong></td>
<td>5,000mm²</td>
<td>4,150mm²</td>
</tr>
<tr>
<td><strong>Standby power</strong></td>
<td>21mW</td>
<td>14mW</td>
</tr>
<tr>
<td>(↓ 17%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Browsing power</strong></td>
<td>1.2W</td>
<td>0.85W</td>
</tr>
<tr>
<td>(↓ 29%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Video</strong></td>
<td>+ 720p encode</td>
<td>+ 1080p encode</td>
</tr>
<tr>
<td><strong>Camera</strong></td>
<td>5 mega-pixel</td>
<td>up to 16 mega-pixel</td>
</tr>
<tr>
<td><strong>Graphics</strong></td>
<td>800 MPPS</td>
<td>2,000 MPPS</td>
</tr>
<tr>
<td>(↑ 250%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Smartphone through the Systems Lens

Design to meet Smartphone cost/power/performance requirements
Medfield System Ingredients

Front

- WIFI/BT Antenna
- Diversity Antenna
- Sensors
- uSD Connector
- eMMC
- Penwell SOC
- 2G/3G Main Antenna
- Modem Memory
- 2G/3G Modem Baseband
- Battery Connector
- HDMI Connector
- LCD Connector
- Power Delivery
- Touch Panel Connector

Rear

- Vibrator
- GPS
- Headset Jack
- SIM Connector
- WIFI Module
- Speaker
- 2G/3G Modem RF
- Rear Camera
- Speaker
Penwell SoC Package Size

- **Memory Peak Bandwidth**
  - 6.4GB/s @ 800MT/s
  - Channels and ranks

- **Dual 32 bit channels**
  - Supports 1 or 2 ranks per channel

- **Memory Size and Density**
  - Supports total memory size of 128MB, 256MB, 512MB and 1GB per channel
  - Supports 1Gb, 2Gb and 4Gb chip

- **Other Features**
  - Aggressive power management to reduce power consumption
  - Proactive page closing policies to close unused pages
  - Supports different physical mappings of bank addresses to optimize for performance

**Package-on-Package (POP)**
- 12 x 12 mm PoP FCMB4 – 32nm
- Non PoP SoC < 0.8 mm
- PoP z height < 1.4mm
- OEM/ODM can solder up to 2 GB of LPDDR2 memory on top of SOC
Medfield with Penwell SOC Block Diagram

LPDDR2

eMMC

SD/MMC

Primary Camera: 8MP, 15fps, 1080p

Secondary Camera: 1.3MP, 1080p

CPU w/512KB L2$

Security Engine

Power Manager

Low Power Audio

2D/3D Graphics

Image Signal Processor

Video Encode/Decode (1080p30)

Display Controller (3 pipes)

Storage

HDMI 1.3a

MIPI-DSI

UART SPI

TI WiFi & BT GPS

HSPA+ Modem

IMC 6260

Power Delivery IC: VRs Audio CODEC USB2 OTG

Rails I2S ULPI

MIPI-HSI

Internal Display

HDMI Display

Penwell SOC (Intel Hi-K 32nm Process Technology)
Penwell CPU Dynamic Dynamic Range

Core Freq = 100MHz
Power: ~50mW

Core Freq = 600MHz
Power: ~175mW

Core Freq = 1.3 GHz
Power: ~500mW

Core Freq up to 1.6 GHz
– for bursty workloads
Power: ~750mW

Ultra-LFM

LFM

HFM

Burst

Fine-grained power management through dynamic voltage & frequency scaling

Core/L2$ Power Is ~Zero
CPU State Saved in SRAM <100 uS Exit Latency

Core Freq = 1.3 GHz
Power: ~500mW

Core Freq up to 1.6 GHz
– for bursty workloads
Power: ~750mW

Fixed Workload

Bursty Workload

Wide Dynamic Range & Fast Exit Latencies = Big Energy Savings

Power assumptions: Tj=70C. Steady State Worst Case ST App Power Projected on Intel 32nm process

Mobile and Communications Group
**Browser Results Summary**

<table>
<thead>
<tr>
<th></th>
<th>P0</th>
<th>600 MHz</th>
<th>900 MHz</th>
<th>1,500 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1x</td>
<td>1.5x</td>
<td>2.5x</td>
<td></td>
</tr>
<tr>
<td>Performance</td>
<td>1x</td>
<td>1.41x</td>
<td>2.24x</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>1x</td>
<td>1.29x</td>
<td>1.81x</td>
<td></td>
</tr>
<tr>
<td>Energy</td>
<td>1x</td>
<td>0.92x</td>
<td>0.81x</td>
<td></td>
</tr>
</tbody>
</table>

“Race to Idle” at higher frequency uses more power, but is lower energy
## Power C-States

<table>
<thead>
<tr>
<th></th>
<th>C0 HFM</th>
<th>C0 LFM</th>
<th>C1/C2</th>
<th>C4</th>
<th>C6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core clock</td>
<td></td>
<td></td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>PLL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1 caches</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2 cache</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wakeup time</td>
<td>active</td>
<td>active</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The OS Is Responsible For Identifying When The Processor Needs To Be In A Certain C State And Requests The Processor To Enter That State
New Platform Level: “S” Ultra Low Power States

S0i1
• Used during idle (e.g. home screen, web browsing)
• Ultra Low Power: mW
• Entry-Exit Latency: $\mu$s

S0i3 / S3
• Used when NOT interacting with the device (e.g. standby mode)
• SoC power: $\mu$W
• Entry-Exit Latency: ms

Achieves Ultra Low Power States with Best-in-Class Latency
CPU Active

Active system looks like this

- Security Engine
- Power Manager
- Low Power Audio
- Storage
- CPU w/512KB L2$
- 2D/3D Graphics
- Video Encode/Decode (1080p30)
- Image Signal Processor
- Display Controller (3 pipes)
CPU Off

CPU w/512KB L2$

- Security Engine
- Power Manager
- Low Power Audio
- Storage

- 2D/3D Graphics
- Video Encode/Decode (1080p30)
- Image Signal Processor
- Display Controller (3 pipes)

CPU is now off!
S0i3/S3 System State

Standby State – just waiting for wakes
New OS Power Management (OSPM)

- Pervasive Power Management
  - Integrated PMU
  - Dedicated Power Delivery IC
  - Active management through HW, FW, SW

- Software-Directed
  - Operating system power management
  - Manages all hardware capabilities

- Fine Grain Power Management
  - 13 rails for IO & logic voltages
  - 45 Power islands for sub-systems
  - Aggressive power and clock gating
  - Integrated clocks and VR power down

OSPM Directs Entire Platform to Lowest Power State
Platform Power Management Architecture

Android Power Manager

Android Power Management Kernel
- Linux PM
- Wakelocks
- Early Suspend

Firmware
- PMU Driver
  - PMU Idle handler
  - PMU Interface
  - Memory Mapped Registers

Kernel Level
- Generic CPU IDLE infrastructure
- Intel Processor / System Driver
  - Idle Handler
- Generic CPU Performance Mgmnt
- Intel CPU Performance Mgmnt

User Level
- PMU Firmware
- PCI_PM
- Runtime PM
- PM_QOS
- Thermal Driver
- Battery Driver
- Graphics Driver
- Device Drivers
Medfield Reference Platform

**High Performance CPU**
1.6 Ghz Intel® Atom™ Processor Z2460

**Full HD Video**
1080p, 30fps Video Encoding
1080p, 30fps Video Playback

**Advanced Imaging**
Intel Image Signal Processing (ISP)
Advanced UI/UX from Intel

**Great Graphics**
PowerVR SGX 540 @ 400 MHz

**High Speed Connectivity**
Intel XMM 6260 21/5.8Mbps HSPA+

**Apps**
Google* Play (Android* Apps)

**High Resolution Display**
Internal: 1024x600; 1024x768p capable
External: 1920x1080 p30 & i60

**Optimized Android Support**
Customizable User Experience

**Enhanced Power/Batterylife**
Standby: 14 days**
Video (1080p): 6 hours
Browsing 3G: 5 hours
Voice Call: 8 hours

**Security**
Programmable Security Engine
Remote Management Features

**Operating System**
Android 2.3.7 (Gingerbread)
Android 4.0.4 (Ice Cream Sandwich)

**Current Design Wins**
Lava XOLO X900 in India
Lenovo K900 in China
Orange San Diego in UK
Orange with Intel Inside® in France.

* other brands and names may be claimed as the property of others
** Battery: 1500mA, 3.7V
All products, designs, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing.
Medfield Summary

• Medfield meets tight Smartphone power consumption constraints and provides outstanding scalar CPU performance
  ✓ “Race to Idle” minimizes energy consumption while providing excellent end-user experience
  ✓ Ultra low power SOC states cater to common “user idle” and “system idle” scenarios
  ✓ Accelerators for Video, Camera, Audio processing provide energy optimized media capabilities