Roadmap for Design and EDA Infrastructure for 3D Products

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## Some of the Typical 3D Options

<table>
<thead>
<tr>
<th>2.5D</th>
<th>Side by side die stacked on a passive interposer that includes TSVs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3D Memory</strong></td>
<td>Multiple DRAM die stacked standalone or on an active interposer</td>
</tr>
<tr>
<td><strong>3D Memory on Logic</strong></td>
<td>One or More DRAM die stacked directly on logic die (M-0-L)</td>
</tr>
<tr>
<td><strong>3D Logic on Logic</strong></td>
<td>Multiple logic die stacked on top of each other (L-o-L)</td>
</tr>
<tr>
<td><strong>3D + Interposer</strong></td>
<td>Mix of side by side and stacked schemes with a passive or active interposer</td>
</tr>
</tbody>
</table>
Evolving to “Mainstream” 3D Technologies

- For 3D stacking
  - e.g. Wide IO Memory on Logic
  - stacking orientation: F2B
  - TSV via diameter ~ 5μ
  - wafer thickness ~ 50
  - uBump Array pitch: 40x50
# Snapshot of Intrinsic Technology Status

<table>
<thead>
<tr>
<th>Process</th>
<th>Was (common concern a few years ago)</th>
<th>Is (our take)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High aspect ratio (10:1) 5/50 TSV process</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Thinning &amp; Backside wafer processing</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Microbump and Joining</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Integration &amp; Stacking</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Intrinsic Reliability Assessment</td>
<td>✹ in flight</td>
<td></td>
</tr>
<tr>
<td>Standards (JEDEC, SEMI, Sematech, 3D EC, …)</td>
<td>✹ in flight</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Design (M-o-L)</th>
<th>Was (common concern a few years ago)</th>
<th>Is (our take)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDA tools (for “2D-like” Memory-on-Logic design)</td>
<td>✹ mostly</td>
<td></td>
</tr>
<tr>
<td>Design Enablement (for “2D-like” Memory-on-Logic design)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Testability (for “2D-like” Memory-on-Logic design)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Variability (Corner for “2D-like” Memory-on-Logic design)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Standards (JEDEC, Si2, IEEE …)</td>
<td>✹ in flight</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Product</th>
<th>Was (common concern a few years ago)</th>
<th>Is (our take)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Level Value Proposition</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Thermal Modeling &amp; Design for Thermal</td>
<td>✹ in flight</td>
<td></td>
</tr>
<tr>
<td>Stress Modeling &amp; Design for Stress</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>SI modeling &amp; Design for Parametric Yield</td>
<td>✓ in flight</td>
<td></td>
</tr>
<tr>
<td>Cost Structure &amp; Business Models</td>
<td>✹ TBD</td>
<td></td>
</tr>
<tr>
<td>Yield and Yield Learning</td>
<td>✹ TBD</td>
<td></td>
</tr>
<tr>
<td>Volume Manufacturing Ramp</td>
<td>✹ TBD</td>
<td></td>
</tr>
</tbody>
</table>
Eco-System for 3D Design

- Segment Design Eco-System into 3 Buckets to Address 3 Key Challenges
  - **Design Authoring** – actual chip design
    - Implement Design via (mostly) Traditional 2D Chip Design Flow (RTL2GDS))
    - Output GDS
  - **PathFinding** – design/technology concept exploration
    - *Manage Choices* via Cheap, Quick & Dirty Concept Design
    - Output Clean Specs
  - **TechTuning** – physical space exploration
    - *Manage Interactions* via Cheap, Electrical, Thermal & Mechanical Chip Simulation
    - Output Clean Constraints
PathFinding: Why & What?

- Managing Choices ….
  - Want to optimize product attributes
  - Cost, power, performance, engineering …
- Need to Co-Optimize Process & Design
  - Winning 3D Product will Be Architected specifically to Leverage 3D Technology
  - Selection of choices is Product Specific
- In General: Need Spatial Awareness
  - Quick and flexible
  - Hi fidelity vis-a-vis accuracy
- For 3D: Also Need Heterogeneity
  - Multiple stacking styles & orientations
  - Multiple tech files
  - Multiple levels of hierarchy
  - Multiple resource constraints
- Structured Methodology.
  - Past experience not applicable
  - Opportunity for paradigm shifts
  - Not tied to Legacy design
  - Process-Design-Package co-optimization
PathFinding

- **Level 1 (Atrenta):** think
  - RTL & Netlists
  - Block Level Schematics
  - Partitions
  - Block assignments
  - T2T connectivity
  - Global Routing
  - Floorplans

- **Level 2 (MicroMagic):** think
  - Transistor Level Schematics
  - T2T layout
  - SPICE Netlist
  - Waveforms
  - Polygons
  - GDS
TechTuning: Why & What?

- Managing Interactions
  - Intimate Proximity and Coupling Between Die
  - In Electrical, Thermal & Mechanical Domains

- Electrical Domain Interactions
  - Within Die Interactions with New Features
    - Substrate noise, Coupling etc..
  - Die to Die interactions (SI, PDN, PI…)

- Thermal Domain Interactions
  - Within a Die & Die to Die
  - Need Thermal Rules & Guidelines
    - Design Specific & Technology Specific
    - Need a methodology to plug into std design flow

- Stress Domain Interactions
  - Within a Die & Die to Die
  - Need Stress Rules & Guidelines
    - Design Specific & Technology Specific
    - Need a methodology to plug into std design flow

Details: 3D IC Stacking Technology, McGraw Hill 2011
3D Electrical Interactions

- Many Possible Interactions
  - Die to Die – close proximity
  - Within a Die – new features

- New Geometries: not just simply planar
  - uBump to BRDL
  - TSV to BRDL
  - TSV to TSV
  - TSV to M1

- New Features: not just conductor or insulator
  - MOS nature of TSV & Semiconductor nature of Si
  - e.g. Substrate Noise Coupling: TSV to Device
    - vs. substrate thickness
    - vs. Doping Profile in the Si substrate
    - vs. TSV to Device Separation
    - vs. Substrate Tap & Guard Ring Configuration
    - etc…

- **Need true 3D Chip Level Extraction & Coupling Analyses**
  - Or a restricted layout with pre-characterized macro model
Thermal Challenges => a Fundamental Constraint

- Thermal: a Global (=System Level) & Local (=Component Level) Challenge
  - Global Concern: must manage skin temperature and overall system power
  - Local Concern: must manage hot spots, junction temperature, and power density
  - Compounding Factor: all advanced systems use some form of Thermal Mitigation

- Thermal is not a 3D-only Challenge
  - A Problem that has to be addressed with 2D Components as well…
  - At Architecture, Design, Floorplanning, Packaging, Application, Software …
  - Could be a 3D Opportunity?

- Need a System-Chip Co-Design Methodology & Tools
  - Faster and More Flexible than the traditional CFD / FEA methodologies
  - Compatible with cross – company handshake (a la TDP practice in PC domain)
  - Compatible with fuzzy PathFinding-like forward looking inputs
  - Compatible with different system level ‘knobs’
  - Compatible with different chip level ‘knobs’

![Diagram showing 2D vs. 3D thermal performance](image-url)
Implementation of a TechTuning Flow for Stress

- Interface to actual Design Authoring: **Rules now**
  - maybe in-flow model based simulation later..
  - Based on ‘off-line’ simulations using specialized tools
  - Define a ‘Safe Operating Area’ => a set of rules
  - Supplement with a smart ‘hot spot’ checker to close the loop

**Traditional Simulation**
- FEA methodology
- ~1 to 0.01mm range
- Hosted Model from AMKOR
- Working on similar deliverable from ASE

**Specialized Simulation**
- Submodeling & specialized FEA methodology
- μm to nm range
- SNPS FAMMOS tool

**“Hot Spot” Checker**
- Validation that bits and pieces fit & SIGN OFF the design
- Must interface to design environment: I/P: GDS2, LEF, DEF ...
- May have to be COMPACT MODEL Based (read the whole design and include all effects)
- Working with MENT
Managing Costs: What Does It Mean for TSS Design?

- Expect Gradual and Graceful Evolution
  - Process and Design – together / in synch
  - Significant investment in the existing flow
  - Will be Applications Driven

- Now: Heterogeneous Stacking
  - e.g. Memory (or Std Analog) on logic
  - Design Methodology Requirements
    - Partitioning: by die types w/ specific interface
    - Syntheses: 1-die-at-a-time
    - Floorplanning: constraint from the other die
    - Physical Design: partial 2-sided die (maybe)
    - Physical Verification: 1-die-at-a-time + interface
    - Analyses: whole stack (e.g. PDN)

- Next: Integrated Stack Designs
  - e.g. Logic-on-Logic or Interposers
  - Design Methodology Requirements
    - Integrated PD Co-Design w/ Interposer & Substrate
    - Design Constraint Methodology
    - Design Authoring – including the Package
    - Manufacturability (aka TechTuning)
3D PDN Design Flow

- **2D Ref Flow**
  - Sign off in time domain (Apache)
  - Analyses in frequency domain (Sigrity)

- **3D PDN Flow Approach**
  - Take as much as possible from ref flow
  - Similar approach as Si-Package-PCB Analyses
    - Extract each tier separately
    - Model as an integrated stack
  - Upgraded tools to understand new features
    - TSV, uBump, BRDL, Tier n ...

- **Current Status**
  - Demonstrated Tools & Flow
  - Supporting development of standard Compact PDN Models and associated 3D Design Exchange Format Standards
## Inventory of Current Core Design Technologies

<table>
<thead>
<tr>
<th>Things We Do Have</th>
<th>PathFinding</th>
<th>TechTuning</th>
<th>Design Authoring</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ 3D Floorplanner</td>
<td>✓ Package Stress simulator</td>
<td>✓ 2D design flow &amp; tools</td>
<td></td>
</tr>
<tr>
<td>✓ 3D Net generator</td>
<td>✓ Feature Stress simulator</td>
<td>✓ Timing with a fixed TSV/uBump layout</td>
<td></td>
</tr>
<tr>
<td>✓ PDN resource estimator</td>
<td>✓ Reference Thermal sim.</td>
<td>✓ 3D aware PI / SI analyses</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Things We are Working On</th>
<th>PathFinding</th>
<th>TechTuning</th>
<th>Design Authoring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package PathFinder</td>
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<tr>
<td>System PathFinder</td>
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<tr>
<td>Standard 3D design exchange formats</td>
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<tr>
<td>Chip Level Stress Sim</td>
<td></td>
<td></td>
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<tr>
<td>Chip thermal floorplanner</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard 3D design exchange format &amp; PDK</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Things we do NOT Have (and wish we did)</th>
<th>PathFinding</th>
<th>TechTuning</th>
<th>Design Authoring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology PathFinder</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>3D in flow substrate coupling analyse</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fully supported TechTuning “PDK’</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System component thermal co-design</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBD Logic on Logic</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBD Interposer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBD 3D Extraction</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBD 3D ++ (see below)</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

- We don’t have Everything – but we do have much more than Nothing 😊!!
Standards: a Lubricant for the Supply Chain

- **Leverage Existing Standards Bodies**
  - Established balloting, adoption and management practices
  - But formal and hence need ‘mature proposals’….

- **Process Standards**
  - 3D Enablement Center
  - Sematech
  - SEMI …

- **Design Standards**
  - Si2
  - 3D EC / SRC
  - IEEE
  - JEDEC…

- **Encourage Participation by the Industry – esp EDA**

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**Product Drivers**

- **3D EC**
  - Sematech
  - 3D Enablement Center
  - Si2 / SRC
  - 3D EC

- **Design Standards**
  - Si2
  - 3D EC

- **Process Standards**
  - SEMI

- **EDA**
- **OSAT**
- **Consortia**
- **SRC**
  - Academia
  - others

- **Process Standards in 2011**
- **Design Standards in 2012**
2.5D / 3D Stacking Roadmap

**Our Current Focus**: Wide IO DRAM on Logic = TSS

**Next**: Logic on Logic / Interposer / Both …

- **TSS Logic on Logic**
- **TSS WideIO Memory on Logic**
- **Interposer Heterogeneous**
- **TSS Everything**
- **Not-Phone driven**
- **Vertical Stacking**
- **Side by Side Stacking**

**In Production**: POP

**3D Integration Levels**

- **W/B & FC Bump Stacking**
- **LPDDRx on Logic**
- **POP**
## Design Environment for Memory-on-Logic

<table>
<thead>
<tr>
<th>Status</th>
<th>Arena</th>
<th>Item</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Have</strong></td>
<td><strong>Design</strong></td>
<td>✓ 2D design flow &amp; tools</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ quasi-manual placement of T2T / TSV array</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ custom T2T buffer design &amp; incremental rules to manage interactions</td>
</tr>
<tr>
<td></td>
<td><strong>Timing</strong></td>
<td>✓ 2.5D analyses flow &amp; tools</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ compound ‘lumped’ TSV delay model</td>
</tr>
<tr>
<td></td>
<td><strong>PI</strong></td>
<td>✓ 2D analyses flow and tools</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ extended hierarchy + recognition of new features</td>
</tr>
<tr>
<td></td>
<td><strong>SI &amp; Variability</strong></td>
<td>✓ ‘Off Line’ analyses to produce set of ‘keep out’ rules</td>
</tr>
<tr>
<td><strong>In Flight</strong></td>
<td><strong>‘In Line’ Rule Checkers</strong></td>
<td>✓ Chip Level Stress Simulator – for ‘stress Hot Spots’</td>
</tr>
<tr>
<td></td>
<td></td>
<td>✓ Chip Level Thermal Floorplanner</td>
</tr>
<tr>
<td></td>
<td></td>
<td>✓ Chip Level SI Simulator</td>
</tr>
<tr>
<td><strong>Integration w/ Commercial Die</strong></td>
<td></td>
<td>✓ 3D Design Exchange Formats</td>
</tr>
<tr>
<td><strong>Like to Have</strong></td>
<td><strong>SI Analyses</strong></td>
<td>☢ In Flow SI analyses – on line and in product flow</td>
</tr>
<tr>
<td></td>
<td><strong>TechTuning &amp; PathFinding</strong></td>
<td>☢ Fully supported TechTuning “PDK”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>☢ System-Component thermal co-design</td>
</tr>
</tbody>
</table>
## Design Environment for Interposers

<table>
<thead>
<tr>
<th>Status</th>
<th>Arena</th>
<th>Item</th>
</tr>
</thead>
</table>
| Have           | Design                       | ✓ 2D Layout tools  
    |                               | ✓ 2D Extraction Tools                                                |
| Need to Have   | Extraction                   | 🍓 Integrated 3D Extraction inc. TSV, routing and FRDL/BRDL           |
|                | Signal Integrity            | 🍓 Integrated SI tools inc floating substrate and 3D features         |
|                | Power Integrity             | 🍓 Integrated PI analyses tools & flow                               |
|                | DFT/Test                     | 🍓 Integrated Double Sided Passive Floating Substrate                 |
|                | PathFinding                  | 🍓 Architectural Trade Off Analyses for Value Proposition             |
## Design Environment for Logic on Logic

<table>
<thead>
<tr>
<th>Status</th>
<th>Arena</th>
<th>Item</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Have</strong></td>
<td>Design</td>
<td>✔️ 2D Flow for One Single Sided Die &amp; Technology at a time</td>
</tr>
<tr>
<td></td>
<td>PathFinding</td>
<td>✔️ 3D Physical PathFinding Flow for finding Value Proposition</td>
</tr>
<tr>
<td><strong>Must Have</strong></td>
<td>Floorplan</td>
<td>⚫ 3D with optimization across multiple tiers (technologies)</td>
</tr>
<tr>
<td></td>
<td>Utility Insertion</td>
<td>3D tools for global utilities – eg NoC, Clock, DFT….</td>
</tr>
<tr>
<td></td>
<td>Extraction</td>
<td>⚫ 3D Extraction inc. TSV, routing and FRDL/BRDL</td>
</tr>
<tr>
<td></td>
<td>Timing</td>
<td>⚫ across multiple tiers, technologies, libraries….</td>
</tr>
<tr>
<td></td>
<td>Power Integrity</td>
<td>Integrated PI analyses tools &amp; flow</td>
</tr>
<tr>
<td></td>
<td>Signal Integrity</td>
<td>in flow SI analyses tools inc 3D features</td>
</tr>
<tr>
<td></td>
<td>DFT / Test</td>
<td>⚫ Optimized DFT overhead for pre-stack test</td>
</tr>
<tr>
<td></td>
<td>Verification</td>
<td>⚫ 3D Physical Verification, LVS, etc across multiple tiers</td>
</tr>
<tr>
<td></td>
<td>etc..</td>
<td>⚫ dependent on the actual stack partition</td>
</tr>
</tbody>
</table>
Thank You