Optical Backplanes with 3D Integrated Photonics?

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Overview

1. Electrical vs. Optical Backplanes
2. Optical vs. Optical Backplanes
3. Chip Stacking: a Means to an End

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100Gbps-m Electrical-to-Optical Crossover

- Data Rate (Gbps)
- Reach

1000
100
10
1
0.1
0.01

10cm 1m 10m 100m 1km 10km 100km
Packages Backplanes Cables Chassis Data Centers Campus/Metro Long-haul

- Backplanes
- 10GSFP+Cu
- Thunderbolt
- 10GBASE-T
- 1000BASE-T
- ADSL2+

*1Gbps over 4 copper wire pairs bidirectionally, effectively 0.5Gbps for each wire pair over a maximum distance of 100m (1000BASE-T spec limit)
100Gbps-m Electrical-to-Optical Crossover

This crossover is not theoretical. It represents 30 years of commercial decisions.

Data Rate (Gbps)

1000
100
10
1
0.1
0.01

Reach

10cm 1m 10m 100m 1km 10km 100km

Packages Backplanes Cables Chassis Data Centers Campus/Metro Long-haul

Backplanes 10GSFP+Cu 10BASE-SR,OM3 100BASE-ER

100BASE-LR4 100BASE-ER4

100BASE-T

Thunderbolt

1000BASE-T

Optical Audio

ADSL2+

Electrical Link

Optical Link

• 1Gbps over 4 copper wire pairs bidirectionally, effectively 0.5Gbps for each wire pair over a maximum distance of 100m (1000BASE-T spec limit)
The Industry Has Managed to Double Backplane Line Rates Every Two Nodes

<table>
<thead>
<tr>
<th>Backplane Transceiver</th>
<th>Sample Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>180nm</td>
<td>3.125Gbps</td>
</tr>
<tr>
<td>130, 90nm</td>
<td>12.5Gbps</td>
</tr>
<tr>
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<tr>
<td>28, 20nm</td>
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<tr>
<td>14, 10nm</td>
<td>100Gbps</td>
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</tbody>
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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes

1. Package Pin-Out Crisis
   Parallel-to-Serial IOs

- 180nm 3.125Gbps
- 130, 90nm 12.5Gbps
- 65, 40nm 25Gbps
- 28, 20nm 50Gbps
- 14, 10nm 100Gbps

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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes

1. Package Pin-Out Crisis
   Parallel-to-Serial IOs

2. Smaller BPs, cabled BPs, active connectors, non-NRZ signaling, etc?

Backplane Transceiver Sample Availability

<table>
<thead>
<tr>
<th>Year</th>
<th>Line Rate (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>180nm 3.125Gbps</td>
</tr>
<tr>
<td>2003</td>
<td>130nm 90nm 12.5Gbps</td>
</tr>
<tr>
<td>2005</td>
<td>65nm 40nm 25Gbps</td>
</tr>
<tr>
<td>2007</td>
<td>28nm 20nm 50Gbps</td>
</tr>
<tr>
<td>2009</td>
<td>Now 100Gbps</td>
</tr>
<tr>
<td>2011</td>
<td>14nm 50Gbps</td>
</tr>
<tr>
<td>2013</td>
<td>Node X, Node Y 100Gbps</td>
</tr>
<tr>
<td>2015</td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td></td>
</tr>
<tr>
<td>Year A</td>
<td></td>
</tr>
<tr>
<td>Year B</td>
<td></td>
</tr>
</tbody>
</table>

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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes

1. Package Pin-Out Crisis Parallel-to-Serial IOs
2. Smaller e- BPs, cabled BPs, active connectors, non-NRZ signaling, etc?
3. BPs hit 100Gbps-m crossover near end of decade?
Electrical vs. Optical Backplanes

Electrical Backplane

Card 1

Backplane

Card 2

Electrical

Electrical

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Electrical vs. Optical Backplanes

Electrical Backplane

Reduce maximum link loss
Electrical vs. Optical Backplanes
Electrical vs. Optical Backplanes

Optical Backplane

Card 1

Integrated Photonics

Card 2

Backplane

Optical

Optical
Optical vs. Optical Backplanes (MMF vs. SMF)

VCSELs: the Incumbent at 10 Gb/s

10Gb/s VCSELs over OM3 MMF
Optical vs. Optical Backplanes

Challengers at 25 Gb/s

- 25Gb/s Si or InP Photonics over SMF for Warehouse Data Centers
- 10Gb/s VCSELs over OM3 MMF
- 25Gb/s VCSELs over OM4 MMF

Reach (km):
- Short Reach
- Medium Reach (Not yet standard)
- Long Reach
Optical vs. Optical Backplanes
Options in Stacked Photonics

VCSELs: Laser is Thermal Bottleneck
70°C 850nm MMF to 90°C 1550nm SMF?

Off-Package Optical Power Supply
Evict thermal bottleneck (laser) from package.

VCSELs Co-Packaged with Logic

- Logic IC (Expensive to cool)
- VCSEL, PD, Driver, Amp ICs

Si or InP Photonics Co-Packaged with Logic

- Logic Package
- Logic IC (100°C OK)
- “Laserless” Photonic ICs (100°C OK)

Which technology will scale better?

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Stacking Photonics
Who faces up and who faces down?

- Photonics up for fiber attach
- Electronics down and with optical vias (holes)

- Photonics down for PWB
- Electronics down
- Si interposer with holes

Integrated-Photonics Interface Standards

Example Today: CEI-28G-VSR

Standard applies to all compliant optical modules, regardless of underlying photonics

Common electrical inter-IC signaling standard
What Happens Outside the Chip Matters

Link loss at connectors: Distance-Cost Trade-offs
Opto-Electronics Supply Chain Needed

Xilinx Stacked-Silicon Supply Chain

- FPGA, Interposer, & Package Design
- 28nm FPGA & Interposer
- Package Substrate
- μBump, Die separation
  CoC/CoWoS, & Assembly
- Final Test of Packaged Part

Opto-Electronics Design

- [Names Here]

Opto-Electronics OSAT

- [Names Here]
Summary

1. Electrical vs. Optical Backplanes
   *Mainstream backplanes to reach crossover near end of decade*

2. Optical vs. Optical Backplanes
   *Choice of VCSELs, InP, and Si Photonics impacts costs & scalability*

3. Chip-stacking is just a means to an end
   *Electrical-to-optical migration: focus on systems and supply chain*