5th Generation Touchscreen Controller for Mobile Phones and Tablets

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Design Goals

- Quick design of derivatives
  - Platform-based design
  - Scalable analog front-end (AFE)
  - Scalable DSP datapath
  - Flexible hardware platform

- Superior noise suppression performance
  - Display noise: DCV com, AC Vcom, OLED
  - Finger-couple noise (charger noise): > 40 Vpp

- Innovation acceleration thru flexible hardware
  - Glove and hover support
  - Robust water rejection and wet finger tracking
  - Passive stylus support
  - Active stylus support
Architectural Elements (I)

- **CPU**
  - Cortex M0 @ 48 MHz
  - Support for flash memory (scalable)
  - Support for SRAM (scalable)
  - Support for ROM memory (scalable)

- **Low-power microcontroller infrastructure**
  - Support for Hibernate, Deep-sleep, Sleep, Idle and Active modes
  - On-chip power generation (LDO and voltage pump)

- **Robust analog front-end (AFE)**
  - Large on-chip integration capacitors
  - Signal attenuators in each channel
  - Large charge handling capability: > 240 pC per cycle
  - High-speed operation: up to 1 Msps
Architectural Elements (II)

- High-voltage signal generation
  - On-chip charge pump for 10V generation

- Configurable DSP datapath
  - Low-power linear and non-linear filtering
    - FIR and window filters
    - Median filtering
  - Digital quadrature demodulation for active stylus
  - Real-time noise-metrics
  - 2D image processing algorithms: filtering, peak-search, etc.

- Table-driven sequencer
  - Flexible timing generation enables advanced scanning modes
  - Easy integration with DDI ASICs for in-cell and on-cell integration
Gen5 Architecture Overview
TSG5_L Touchscreen Controller

- ARM CM0
- ARM Debug
- Low power
- CY S8 Process
  - 130nm
  - FLASH
  - 10V capable
TSG5 RX AFE Architecture

Per-edge signal processing, 40V charger noise
Gen5: Application of Flexible Timing Generation

- D67 = integrate for 2/3 of the period, or 67% duty cycle
  - Removes 3rd/6th/9th harmonics, e.g. for $F_{TX}=100\text{kHz}$ that’s 300/600/900kHz
  - Esp. effective for slow panels. 1.5x noise immunity for all the higher-freq noise
## Gen 4/5 Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>Gen 4</th>
<th>Gen 5</th>
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</thead>
<tbody>
<tr>
<td>TX drive (square wave)</td>
<td>2.6-10V</td>
<td>2.6-10V, $C_{ext}$ or $V_{TX}$</td>
</tr>
<tr>
<td>MPTX</td>
<td>4</td>
<td>Full axis</td>
</tr>
<tr>
<td>TX frequency</td>
<td>$\leq 300\text{kHz}$</td>
<td>$\leq 500\text{kHz}$</td>
</tr>
<tr>
<td>Max RX sample rate</td>
<td>$\geq 2$ TX (sub-int)</td>
<td>$\frac{1}{2}$ TX (=per edge)</td>
</tr>
<tr>
<td>HW Baseline Cal.</td>
<td>Yes</td>
<td>Yes, larger</td>
</tr>
<tr>
<td>Max RX charge</td>
<td>8pC/edge</td>
<td>30..200pC/edge</td>
</tr>
<tr>
<td>RX ADC</td>
<td>10b SAR, shared, shared</td>
<td>8b SAR per ch.</td>
</tr>
<tr>
<td>LX channel</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LCD sync</td>
<td>Int/ext</td>
<td>Int/ext</td>
</tr>
<tr>
<td>Signal processing</td>
<td>M0 CPU, 32b</td>
<td>CPU or CE</td>
</tr>
<tr>
<td>Noise metric</td>
<td>CPU</td>
<td>CPU or CE</td>
</tr>
<tr>
<td>Autom. sequencing</td>
<td>Yes</td>
<td>Yes, table driven</td>
</tr>
<tr>
<td>Self &amp; Mutual Cap</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>$V_{DDD}$</td>
<td>1.71 – 5.5V</td>
<td>1.71-5.5V</td>
</tr>
<tr>
<td>$V_{CCA}$ (core)</td>
<td>2.4V</td>
<td>2.65-5.5V</td>
</tr>
</tbody>
</table>
Current Status and Future Developments

- Smartphone and tablet devices available **today**
  - TGS5_M: 36 I/Os and 11 channels, supporting phones up to 4.7”
  - TSG5_L: 58 I/Os and 21 channels, supporting phones and tablets up to 9”

- Large tablet and notebook device available later in the year
Thank You

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